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Paxton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Constantin Bulucea and Rebecca Rossen
Assignee:	Siliconix incorporated
Title:	Trench DMOS Power Transistor With Field-Shaping Body Profile and Three-Dimensional Geometry
Application No.:	08/851,608 — Filed: 5 May 1997
Examiner:	S. Crane — Group Art Unit: 2811
Docket No.:	M-799-4C US

San Jose, California
23 December 2002

BOX CPA
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97(b)

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, the documents listed on the accompanying substitute PTO Form 1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed, including translations where indicated. Copies of English abstracts of all the cited Japanese Patent Publications ("JPPs") are also enclosed, except for JPP 63-124762, a utility model JPP.

The present application is a file-wrapper continuation of parent U.S. patent application 08/453,285 which, in turn, is a file-wrapper continuation of grandparent U.S patent application 08/086,976. Hence all documents cited in parent application 08/453,285 and in grandparent application 08/086,976 are of record in the present application.

JPP 62-12167 was previously cited in grandparent application 08/086,976 and is re-cited here because an English translation of JPP 62-12167 is enclosed.

JPP 62-37965 was previously cited in grandparent application 08/086,976 using the partial number "0037965". JPP 62-37965 is re-cited here for clarity using its full publication

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

number. Also, the JPP 62-37965 publication date, previously given as 15 February 1987, is corrected here to 18 February 1987.

Blanchard, "Optimization of High Power MOS Transistors", was cited in parent application 08/453,285 and is re-cited here to identify the page numbers and indicate that the document is a Ph.D. dissertation.

Katoh et al, "Design of New Structural High Breakdown Voltage V-MOSFET -- Static Shield V-MOSFET", was cited earlier in this application and is re-cited here because a copy of the Japanese version of the document is enclosed.

Ueda et al, "High Speed Power MOSFET, U-MOS Power FET", was cited earlier in this application using the partial title "U-MOS Power FET" and is re-cited here (a) to present the full title and (b) because an English translation is enclosed. Inasmuch as the Japanese version of Ueda et al, "High Speed Power MOSFET, U-MOS Power FET", has two sets of page numbers, both sets of page numbers "335 - 442" and "143 - 150" are included here in the citation rather than the single set of page numbers "143 - 150" previously used in the citation.

Applicants' attorney does not have an English translation of Kato et al, "A Study for High Voltage V-MOS Structure". However, Kato et al, "A Study for High Voltage V-MOS Structure", appears to deal with material similar to that in Katoh et al, "Design of New Structural High Breakdown Voltage V-MOSFET—Static Shield V-MOSFET", and similar to that in Katoh et al, "Design of High Breakdown V-MOSFET Applying Static Shield Effect".

Applicants' attorney recognizes that the enclosed copies of some of the cited documents repeat copies previously provided to the PTO in connection with the present application, with parent application 08/453,285, or with grandparent application 08/086,976. To the extent that such accumulation of multiple copies may be inconsistent with PTO policy or rules, Applicants' attorney requests the Examiner to discard the earlier-provided copies.

Further enclosed to simplify printing of the present application is a Summary of all the Documents Cited, i.e., now of record, in the present application and suitable for being listed on the first page of the patent as "References Cited". In the enclosed Summary of Cited Documents, the citations for some of the journal articles have been simplified by deleting unnecessary material such as the names of authors after the first-named authors.

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25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Siliconix inc. ("Siliconix"), the assignee of the present application, is also the assignee of (a) U.S. Patent 5,072,266, the great great grandparent of the present application, and (b) U.S. Patent 5,298,442, the great grandparent of the present application.

Siliconix sued Fairchild Semiconductor Corp. ("Fairchild") for infringement of U.S. Patents 5,072,266 and 5,298,442. The patent infringement suit, now settled, was brought in the Northern District of California as case no. 99-04797 SBA. In the infringement suit, Fairchild submitted a 66-page Response Chart in which Fairchild alleged that certain claims of U.S. Patents 5,072,266 and 5,298,442 were invalid as anticipated by, or/and obvious in view of, certain references cited in the Response Chart.

A copy of the Response Chart, dated 30 August 2000, is enclosed. Subject to the comments in the next two paragraphs, all of the documents cited in the Response Chart are included with the enclosed substitute PTO Form 1449 or are already of record in the present application including parent application 08/753,285 and grandparent application 08/086,976. Likewise, aside from the documents already of record in the present application, copies of all the documents cited in the Response Chart are included with the enclosed copies of the references cited in the substitute PTO Form 1449.

On page 3 of the Response Chart, the citation to Kato et al, "A Study of High Voltage V-MOS Structure", should apparently be Kato et al, "A Study for High Voltage V-MOS Structure". That is, "of" in the title should apparently be "for".

Page 3 of the Response Chart cites (a) Katoh et al, "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect," IEICE Transactions C, Vol. 66, No. 6, 1983, and then (b) Kato et al, "High Voltage-ization Using Static Shield Effect", Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984. As far as applicants' attorney can determine, these two documents are respective English and Japanese versions of a single reference. Also, the journal/date citation information appears to be wrong for the English version, item (a). Referring to the enclosed substitute PTO Form 1449 and the accompanying copies of the cited documents, items (a) and (b) appear to be Katoh et al, "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect", Review of the Electrical Communications Laboratories (which is probably an alternative English translation of the Japanese journal translated into English as Electrical Communications Laboratories Technical Journal for item b) while the remaining citation information is Vol.

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25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

32, No. 6, 1984, pages 1107-1114, for the English version, and Vol. 33, No. 2, 1984, pages 257-268, for the Japanese version.

In the Siliconix/Fairchild patent infringement suit, Fairchild also submitted an Amended Initial Disclosure of Defendant Fairchild Semiconductor – Prior Art in which Fairchild cited over five hundred references, including references cited in the Response Chart. A copy of this Amended Initial Prior Art Disclosure, likewise dated 30 August 2000, is enclosed.

Certain of the references cited in the Amended Initial Prior Art Disclosure are classified as "102" or/and "103" references with respect to U.S. Patents 5,072,266 and 5,298,442. However, the Amended Initial Prior Art Disclosure does not cite any particular claim(s) of U.S. Patents 5,072,266 and 5,298,442, and does not provide any analogies between any of the claims of U.S. Patents 5,072,266 and 5,298,442, on one hand, and the material of any of the cited references, including the "102", "102/103", and "103" references, on the other hand. All of the "102" references, including three "102" references not mentioned in the Response Chart, are listed on the accompanying substitute PTO Form 1449 or are already of record in the present application.

Aside from the references cited in both the enclosed substitute PTO Form 1449 and the Amended Initial Prior Art Disclosure, Applicants' attorney has not obtained copies of and/or reviewed any of the further references cited in the Amended Initial Prior Art Disclosure in connection with the present application, and expresses no view as to the materiality of any of these further references to any of the claims of this application. The enclosed copy of the Amended Initial Prior Art Disclosure is provided in fulfillment of applicants' attorneys' obligation of candor and good faith with the PTO.

If the Response Chart and the Amended Initial Prior Art Disclosure themselves need to be listed on a (substitute) PTO Form 1449 in order for the Examiner to be obligated to consider these two Fairchild documents, please so inform Applicants' attorney.

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made; or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

Please telephone Applicants' attorney at 408-453-9200, ext. 1371, if there are any questions regarding this submission.

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Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicants
Reg. No. 29,089

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

#20

TERRENCE P. McMAHON (State Bar No. 71910)
WILLIAM L. ANTHONY, JR. (State Bar No. 106908)
MONTE COOPER (State Bar No. 196746)
KAI TSENG (State Bar No. 193756)
THOMAS J. GRAY (State Bar No. 191411)
ORRICK, HERRINGTON & SUTCLIFFE LLP
1020 Marsh Road
Menlo Park, CA 94025
Telephone: (650) 614-7400
Facsimile: (650) 614-7401

Attorneys for Defendant
FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

(OAKLAND DIVISION)

SILICONIX INCORPORATED, a Delaware corporation, Plaintiff, v. FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, Defendant.	CASE NO. 99-04797 SBA **RESPONSE CHART (Civil L.R. 16-9(b))**

Pursuant to Civil Local Rule 16-9(b), Fairchild Semiconductor Corporation ("Fairchild") herein serves its response chart on Plaintiff Siliconix Incorporated ("Siliconix"). Fairchild provides the following claim invalidity analysis under 35 U.S.C. §§ 102 and 103.

I. INTRODUCTION

Local Rule 16-9(a) requires that the party alleging infringement of a patent must submit a claim chart which "must contain" information identifying "where each element of each infringed claim is found within each apparatus, product [or] device . . .". L.R. 16-9(a)(4). Siliconix's claim chart alleges that Claim 1 of U.S. Patent No. 5,072,266 ("the '266 patent")and Claims 17, 18, 19, 20, 22, 23 and 24 of U.S. Patent No. 5,298,442 ("the '442 patent") are infringed by the Fairchild FDS 6680A product. Siliconix has failed to provide a claim chart which applies the asserted claims of the '266 patent and '442 patent against any other Fairchild product.

Accordingly, Siliconix should be precluded from asserting infringement of the '266 patent and/or '422 patent against any other Fairchild product.

II. RESPONSIVE CHART

The following chart indicates which claims of the patent are anticipated by which pieces of prior art. Please note that the information in this document is provisional and subject to revision, for the following reasons:

(i) Fairchild's position on the invalidity of particular claims will depend on how those claims are construed by the Court. Because claim construction has not yet occurred, Fairchild cannot take a final position on the bases for invalidity of disputed claims because the Court may construe those claims to mean something different from what Fairchild presently assumes them to mean.

(ii) Fairchild has not yet completed its search for prior art.

(iii) Fairchild has not completed its discovery from Plaintiff. Depositions of the persons involved in the drafting and prosecution of the patent-in-suit, and of the inventor, for instance, will likely reveal information that affects the conclusions herein.

Fairchild reserves the right to revise and/or supplement the claim chart. Fairchild incorporates herein the prosecution file history of the '266 patent and the '442 patent.

Presently, Fairchild intends to rely upon the following prior art patents and references:

JP 55146976

JP 58137254

JP 62-16572 -

Physics and Technology of Power MOSFETs, Shi-Chung Sun, UMI Dissertation Services, February 1982

Optimization of Discrete High Power MOS Transistors, Richard A. Blanchard, UMI Dissertation Services, Dec. 1981

JP 62012167

U.S. Patent 4,420,379

JP 63-124762

JP 63-224260

JP 59-181668

JP 54-57871

JP 57-72365

JP 59-193064

JP 60-28271

JP 57-18365

JP 59-80970

U.S. Patent 4,345,265

U.S. Patent 4,443,931

U.S. Patent 4,532,534

U.S. Patent 4,374,455

U.S. Patent 4,767,722

U.S. Patent 3,412,297

U.S. Patent 4,783,694

U.S. Patent 4,593,302

Design of New Structural High Breakdown Voltage V-MOSFET – Static Shield V-MOSFET, Kuniharu Katoh and Yuki Shimada, Electronics and Communications in Japan, Vol. 66-C, No. 6, 1983

A Study of High Voltage V-MOS Structure, Kunihara Kato, et al., IEICE Transactions C., Vol. 81, No. 7(ED81-4), 1981.

Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect, Kunihara Kato, et al., IEICE Transactions C, Vol. 66, No. 6, 1983.

High Voltage-ization Using Static Shield Effect, Kunihara Kato, et al., Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984.

U-MOS Power MOSFET, Daisuke Ueda, et al., National Technical Report, Vol. 29, No. 2, Apr. 1983

Fairchild reserves the right to rely upon the prior art patents disclosed in Fairchild's Amended Initial Disclosure of Prior Art after a claim construction is performed by the Court.

Fairchild provides the following claim invalidity analysis under 35 U.S.C. §§ 102 and 103. In the event that any cited prior art is found not to be anticipatory under 35 U.S.C. § 102, Fairchild reserves the right to rely upon the cited prior art to prove obviousness under 35 U.S.C. § 103.

Prior Art Under 35 U.S.C. § 102 Which Anticipates the '568 Patent:

JP 55146976

JP 58137254

JP 62-16572

Physics and Technology of Power MOSFETs, Shi-Chung Sun, UMI Dissertation Services, February 1982

Optimization of Discrete High Power MOS Transistors, Richard A. Blanchard, UMI Dissertation Services, Dec. 1981

JP 62012167

U.S. Patent 4,420,379

JP 63-124762

JP 63-224260

JP 59-181668

JP 54-57871

JP 57-72365

JP 59-193064

JP 60-28271

JP 57-18365

JP 59-80970

U-MOS Power MOSFET, Daisuke Ueda, et al., National Technical Report, Vol. 29, No. 2, Apr. 1983

The Following References (referred hereinafter as "KATOH") Will Be Analyzed Together:

Design of New Structural High Breakdown Voltage V-MOSFET – Static Shield V-MOSFET, Kuniharu Katoh and Yuki Shimada, Electronics and Communications in Japan, Vol. 66-C, No. 6, 1983

A Study of High Voltage V-MOS Structure, Kunihara Katoh, et al., IEICE Transactions C., Vol. 81, No. 7(ED81-4), 1981.

Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect, Kunihara Katoh, et al., IEICE Transactions C, Vol. 66, No. 6, 1983.

High Voltage-ization Using Static Shield Effect, Kunihara Katoh, et al., Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266 CLAIM 1	JP 55146976
1. A trench DMOS transistor cell comprising:	Double Diffusion Insulating Gate Field Effect Transistor
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (101)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer (102)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (3)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (104) the P layer (3) has a heavily doped P+ region (103) which extends upward through the N+ layer (104) and which extends downward (110-1 and 110-2) into the N- layer (102)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (5) with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (104) through the N+ layer (104), the P layer (3) and through a portion of the N- (102) layer, wherein the bottom surface of the trench (5) lies above a lowest part of the downward portion of the P+ region of the P layer.
electrically conducting semiconductor material positioned within the trench;	semiconductor material (107)

a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide (106)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the semiconductor material (107), to the N+ layer (104) and to the N+ substrate (101).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 55146976
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	Double Diffusion Insulating Gate Field Effect Transistor
providing a first region of a first conductivity type;	N+ layer (101) and N- layer (102)
providing a second region of a second conductivity type over said first region;	P layer (3) formed by a first diffusion
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (104) formed by a second diffusion
providing a trench through said third and second regions; and	trench (5) with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (104) through the N+ layer (104), the P layer (3) and through a portion of the N- (102) layer.
providing a gate in said trench;	Al gate electrode (107)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (3) has a heavily doped P+ region (103) which extends upward through the N+ layer (104) and which extends downward (110-1 and 110-2) through the N- layer (102) deeper than the trench (5)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	the P layer (3) has a heavily doped P+ region (103) laterally spaced from the trench (5)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (101) under N- layer (102)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer (102)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide (106)

CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	Double Diffusion Insulating Gate Field Effect Transistor
providing a first region of a first conductivity type;	N+ layer (101)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N- layer (102)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3) formed by a first diffusion
providing a fourth region of said first conductivity type over said third region;	N+ layer (104) formed by a second diffusion
providing a trench through said fourth region and third regions; and	trench (5) with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (104) through the N+ layer (104), the P layer (3) and through a portion of the N- (102) layer.
providing a gate in said trench;	Al gate electrode (107)
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (3) is laterally spaced from said trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (3) and the N+ layer (101) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (102) and the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the P layer (3) is heavier doped (P+ region(103)) than the part of the P layer (3) adjacent trench (5)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**JP 58137254**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	Insulated Gate Semiconductor Device See Fig. 7
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (13)

a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (14); the P layer (13) has a heavily doped P+ region (19) portion which extends upward through the N+ layer (14) and which extends downward into the N- layer (2)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (14) through the N+ layer (104), the P layer (13) and through a portion of the N- (19) layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the P+ region of the P layer.
electrically conducting semiconductor material positioned within the trench;	gate semiconductor material (17)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide insulating film (16)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the gate semiconductor material (17), to the N+ layer (14) and to the N+ substrate (1).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 58137254
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Insulated Gate Semiconductor Device See Fig. 7
providing a first region of a first conductivity type;	N+ layer (1) and N- layer (2)
providing a second region of a second conductivity type over said first region;	P layer (13) formed by a first diffusion
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (14) formed by a second diffusion
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (14) through the N+ layer (14), the P layer (13) and through a portion of the N- (2) layer.
providing a gate in said trench;	gate semiconductor material (17)

wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (13) has a heavily doped P+ region (19) which extends upward through the N+ layer (14) and which extends downward through the N- layer (2) deeper than the trench
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	the P layer (13) has a heavily doped P+ region (19) which is laterally spaced from the trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (1) under N- layer (2)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide insulating film (16)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	Insulated Gate Semiconductor Device
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N- Layer (2)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (13) formed by a first diffusion
providing a fourth region of said first conductivity type over said third region;	N+ layer (14) formed by a second diffusion
providing a trench through said fourth region and third regions; and	V trench which extends vertically downward from the top surface of the N+ layer (14) through the N+ layer (14), the P layer (13) and through a portion of the N- (2) layer.
providing a gate in said trench;	gate electrode (17)
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (13) is laterally spaced from said V trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (13) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (13) at the deepest part of the P layer (13) and which is reverse biased around its breakdown voltage

CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer (13) has a heavily doped P+ region (19) which is laterally spaced from the trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266 CLAIM 1	JP 6216572
1. A trench DMOS transistor cell comprising:	Vertical-type Semiconductor Device and Manufacturing Method Therefore See figs. 1(a) and 1(b)
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (4)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (8) (p. 11 of translation: "Contracted by an n+-type semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short portions underneath the n+-type semiconductor layer 8.") p. 11 of translation: "Forming p+-type semiconductor layers 3 in cells by photolithography is used as another way of reducing the likelihood of the punch-through phenomenon occurring in conventional DSA MOS FETs." the P layer (4) has a heavily doped P+ region (3) portion which extends upward through the N+ layer (1) and which extends downward into the N layer (2)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	p. 12 of translation: "The vertical-type semiconductor device in accordance with the present invention is characterized by comprising a semiconductor substrate of a first conduction type whose principal surface is provided with a groove; a semiconductor film or conductor film pattern formed through the agency of a first insulating film over the groove formed in the principal surface of the semiconductor substrate . . ." As seen from Fig. 1(b), the P layer (4) has a heavily doped P+ region (3) portion which extends upward through the N+ layer (8) and which extends downward into the N layer (2)
electrically conducting semiconductor material positioned within the trench;	source Al electrode 9 is formed on this insulating film p. 12 of translation: ". . . a semiconductor film or conductor film pattern formed through the agency of a first insulating film over the groove formed in the principal surface of the semiconductor substrate . . ."

a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	first insulating film (5a)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	Source Al electrode (9a). Gate Al electrode (9b). Since the device is a vertical-type semiconductor device, the N+ layer (1) must have a drain electrode.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 62-16572
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	Vertical-type Semiconductor Device and Manufacturing Method Therefore See figs. 1(a) and 1(b)
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (4) with a P+ region (3).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (8) (p. 11 of translation: "Contracted by an n+-type semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short portions underneath the n+-type semiconductor layer 8.")
providing a trench through said third and second regions; and	p. 12 of translation: "The vertical-type semiconductor device in accordance with the present invention is characterized by comprising a semiconductor substrate of a first conduction type whose principal surface is provided with a groove; . . . "
providing a gate in said trench;	p. 12 of translation: " . . . a semiconductor film or conductor film pattern formed through the agency of a first insulating film over the groove formed in the principal surface of the semiconductor substrate . . ."
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (4) has a heavily doped P+ region (3) which extends upward through the N+ layer (8) and which extends downward through the N- layer (2) deeper than the groove
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	the P layer (4) has a heavily doped P+ region (3) which is spaced away from the groove
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (1) under N layer (2).

CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	first insulating film (5a)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	Vertical-type Semiconductor Device and Manufacturing Method Therefore See figs. 1(a) and 1(b)
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (2)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (4)
providing a fourth region of said first conductivity type over said third region;	N+ layer (8) (p. 11 of translation: "Contracted by an n+-type semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short portions underneath the n+-type semiconductor layer 8.")
providing a trench through said fourth region and third regions; and	p. 12 of translation: "The vertical-type semiconductor device in accordance with the present invention is characterized by comprising a semiconductor substrate of a first conduction type whose principal surface is provided with a groove; a semiconductor film or conductor film pattern formed through the agency of a first insulating film over the groove formed in the principal surface of the semiconductor substrate . . ." As seen from Fig. 1(b), the P layer (4) has a heavily doped P+ region (3) portion which extends upward through the N+ layer (8) and which extends downward into the N layer (2)
providing a gate in said trench;	p. 12 of translation: "The vertical-type semiconductor device in accordance with the present invention is characterized by comprising a semiconductor substrate of a first conduction type whose principal surface is provided with a groove; . . ." p. 12 of translation: " . . . a semiconductor film or conductor film pattern formed through the agency of a first insulating film over the groove formed in the principal surface of the semiconductor substrate . . ."
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (4) is laterally spaced from said groove.

wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer (4) at the deepest part of the P layer (4) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer (4) has a heavily doped P+ region (3) which is spaced away from the groove

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	Physics and Technology of Power MOSFETs
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VDMOS – see Figs. 2.1, 2.21 and 3.21
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer As seen in Fig. 2.1, a portion of the P layer is heavily doped P+; the P+ region extends vertically upward around the N+ layer and downward into the N- layer
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
electrically conducting semiconductor material positioned within the trench;	semiconductor material
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide between the trench and gate
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the semiconductor material, to the top N+ layer and to the N+ substrate.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**Physics and Technology of Power MOSFETs**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VDMOS – see Figs. 2.1, 2.21 and 3.21
providing a first region of a first conductivity type;	N+ layer substrate and N- layer
providing a second region of a second conductivity type over said first region;	P layer formed by a first diffusion
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer formed by a second diffusion
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
providing a gate in said trench;	Al gate electrode
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer has a heavily doped P+ region which extends upward through the N+ layer and which extends downward through the N- layer deeper than the trench.
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	the P layer has a heavily doped P+ region which is laterally spaced away from the trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer substrate under the N- layer
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide between the trench and gate
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VDMOS – see Figs. 2.1, 2.21 and 3.21
providing a first region of a first conductivity type;	N+ layer
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N- Layer

providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer formed by a first diffusion
providing a fourth region of said first conductivity type over said third region;	N+ layer formed by a second diffusion
providing a trench through said fourth region and third regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
providing a gate in said trench;	Al gate electrode
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer is laterally spaced from said trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer and the N+ layer is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer and the P layer at the deepest part of the P layer and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer has a heavily doped P+ region which is laterally spaced away from the trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	Optimization of Discrete High Power MOS Transistors
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS Structure – see Fig. 4.22
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer; the P layer has a heavily doped P+ region portion which extends upward through the N+ layer and which extends downward into the N layer.
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.

the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	
electrically conducting semiconductor material positioned within the trench;	semiconductor material
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide between the trench and gate
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the semiconductor material, to the top N+ layer and to the N+ substrate.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	Optimization of Discrete High Power MOS Transistors
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VMOS Structure – see Fig. 4.22
providing a first region of a first conductivity type;	N+ layer substrate and N- layer
providing a second region of a second conductivity type over said first region;	P layer formed by a first diffusion
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer formed by a second diffusion
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
providing a gate in said trench;	Al gate electrode
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer has a heavily doped P+ region which extends upward through the N+ layer and which extends downward through the N- layer deeper than the trench.
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	the P layer has a heavily doped P+ region which is laterally spaced away from the trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer substrate under the N- layer

CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer.
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide between the trench and gate
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS Structure – see Fig. 4.22
providing a first region of a first conductivity type;	N+ layer
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N- Layer
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer formed by a first diffusion
providing a fourth region of said first conductivity type over said third region;	N+ layer formed by a second diffusion
providing a trench through said fourth region and third regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
providing a gate in said trench;	Al gate electrode
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer is laterally spaced from said trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer and the N+ layer is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer and the P layer at the deepest part of the P layer and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer has a heavily doped P+ region which is laterally spaced away from the trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 62012167
CLAIM 1	
1. A trench DMOS transistor cell comprising:	Manufacture of Vertical Type Semiconductor Device with Groove Section See fig. 1(f).
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (11) (p. 5 of the translation: "a n+-type semiconductor substrate 11 with a high concentration of impurities is coated with an n-type semiconductor layer 12 having a lower concentration of impurities.")
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (12)

a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (16)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (17) lying partly over the P layer (16) P layer (16) extends vertically upward through the N+ layer (17) to the top surface and downward into the N layer (12)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	p. 6 of translation: " The grooved portion 20 has smooth outlines and does not have any sharp pointed sections." As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends downward into the P layer (16) and the N layer (12)
electrically conducting semiconductor material positioned within the trench;	p. 6 of translation: " . . . polycrystalline silicon film 22 constituting a gate electrode . . ."
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide film (21)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the semiconductor material (22), to the top N+ layer (17) and to the N+ substrate (11).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 62012167
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	Manufacture of Vertical Type Semiconductor Device with Groove Section See fig. 1(f).
providing a first region of a first conductivity type;	N+ layer (11) and N layer (12).
providing a second region of a second conductivity type over said first region;	P layer (16).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (17) lying above the P layer (16).
providing a trench through said third and second regions; and	p. 6 of translation: " The grooved portion 20 has smooth outlines and does not have any sharp pointed sections." As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends downward into the P layer (16) and the N layer (12)
providing a gate in said trench;	gate oxide film (21)

wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (16) extends upward through the N+ layer (17) and which extends downward through the N layer (12) deeper than the grooved portion (20)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	N/A
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ substrate (11) under N layer (12)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N layer (12)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide (21)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	Manufacture of Vertical Type Semiconductor Device with Groove Section See fig. 1(f).
providing a first region of a first conductivity type;	N+ layer (11)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (12)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (16)
providing a fourth region of said first conductivity type over said third region;	N+ layer (17) lying above the P layer (16)
providing a trench through said fourth region and third regions; and	p. 6 of translation: " The grooved portion 20 has smooth outlines and does not have any sharp pointed sections." As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends downward into the P layer (16) and the N layer (12)
providing a gate in said trench;	gate oxide film (21)
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (16) is laterally spaced from said groove.

wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (16) and the N+ layer (11) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (12) and the P layer (16) at the deepest part of the P layer (16) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	N/A

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

- U.S. Patent 5,072,266	U.S. Patent 4,420,379
CLAIM 1	
1. A trench DMOS transistor cell comprising:	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Self-Aligned, Non Planar, MOS Transistor See Figs. 3-19.
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (20)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer (21)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (22), (25) and (27)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (26) the P layer has a heavily doped P+ region (22) which extends upward through the N+ layer (26) and which extends downward into the N- layer (21) Col. 4, lns. 23-26: "In the stage shown as FIG. 5, the device undergoes an oxidizing treatment which simultaneously deepens the P+ type guard ring and protects the peripheral part of the junction under a thick oxide layer 23 (1 micron), called the field oxide."
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (30) with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (26) through the N+ layer (26), the P layer (25) and through a portion of the N- (21) layer, wherein the bottom surface of the trench (30) lies above a lowest part of the downward portion of the P layer (22)
electrically conducting semiconductor material positioned within the trench;	semiconductor material (32)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide (31)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate semiconductor material (32), source electrode (33) and drain at N+ substrate (20)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	U.S. Patent No. 4,420,379
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Self-Aligned, Non Planar, MOS Transistor See Figs. 3-19.
providing a first region of a first conductivity type;	N+ layer (20) and N- layer (21)
providing a second region of a second conductivity type over said first region;	P layer (22), (25) and (27)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (26)
providing a trench through said third and second regions; and	trench (30) through the N+ layer (26), the P layer (25) and through a portion of the N- (21) layer
providing a gate in said trench;	gate semiconductor material (32)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion of the P layer (22), which portion is spaced from the trench (30), extends deeper than the trench (30) a portion of the P Layer (22) acts as a guard rail to spread the electric field at the periphery and away from the channel.
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	P layer has a heavily doped P+ portion (22) which is laterally spaced from the trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (20) under N- layer (21)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer (21)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide (31)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Self-Aligned, Non Planar, MOS Transistor See Figs. 3-19.
providing a first region of a first conductivity type;	N+ layer (20)

providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N- layer (21)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (22), (25) and (27)
providing a fourth region of said first conductivity type over said third region;	N+ layer (26)
providing a trench through said fourth region and third regions; and	trench (30) through the N+ layer (26) and the P layer (25) and through a portion of the N- (21) layer
providing a gate in said trench;	gate semiconductor material (32)
wherein a deepest part of said third regions is laterally spaced from said trench;	the P layer region (22) is laterally spaced from trench (30)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (22) and the N+ layer (20) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (21) and the P layer (22) at the deepest part of the P layer (22) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the third region is P+ and is doped heavier than the part of the third region P (25) adjacent the trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 63-124762
CLAIM 1	
1. A trench DMOS transistor cell comprising:	Vertical MOSFET See fig. 1
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (3), (11) and (12)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (4) lying partly over the P layer (3) A portion of the P layer (11) and (12) is heavily doped P+ and extends upward through the N+ layer (4) to the top and downward into the N layer (2).
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer	trench (8) having a bottom surface and side surfaces and extending vertically downward from the top surface of the N+ layer (4) through the N+ layer (4) and the P layer

and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	(3) and through a portion of the N layer (2), wherein the bottom surface of the trench (8) lies above a lowest part of the P+ layer (12)
electrically conducting semiconductor material positioned within the trench;	trench (8) possess a highly doped poly-silicon gate electrode (9)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide film (7)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate electrode (9), source electrode (14) and drain electrode (15)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 63-124762
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Vertical MOSFET See fig. 1
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2)
providing a second region of a second conductivity type over said first region;	P layer (3), (11) and (12)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (4) such that P layer (3) is between the N layer (2) and the N+ layer (4)
providing a trench through said third and second regions; and	trench (8) extending through the N+ layer (4) and the P layer (3)
providing a gate in said trench;	trench (8) possess a highly doped poly-silicon gate electrode (9)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	portion P+ (12) is spaced from trench (8) and extends deeper than said trench (8) so that, if a predetermined voltage is applied to the gate (9) and to N+ layer (4) and another predetermined voltage is applied to the N+ layer (1), an avalanche breakdown occurs away from a surface of the trench (8).
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	A portion of the P layer (11) and (12) is heavily doped P+ P layer (3) is adjacent the trench (8)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (1) under N layer (2)

CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide film (7)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	Vertical MOSFET See fig. 1
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (2)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3), (11) and (12) over N layer (2)
providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (3).
providing a trench through said fourth region and third regions; and	trench (8) through N+ layer (4) and P layer (3)
providing a gate in said trench;	gate oxide film (9)
wherein a deepest part of said third regions is laterally spaced from said trench;	portions of P layer (11) and (12) are laterally spaced from trench (8)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (12) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (12) at the deepest part of the P layer (12) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the third region is P+ (12) and is doped heavier than the part of the third region P (3) adjacent the trench (8)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 63-224260
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET See fig. 1
a substrate of semiconductor material of heavily doped first electrical conductivity type;	P layer (11) (opposite conductivity type with respect to drain).
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer (12)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (13) (20) lying on N layer (12)

a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (14) lying partly over the P layer (13), wherein a portion of the P layer (20) is heavily doped P+ and extends downward into the N- Layer (12)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (15) having a bottom surface and side surfaces and extends vertically downward from the top surface of N+ layer (14) through the N+ layer (14) and the P layer (13) and through a portion of the N- layer (12), wherein the bottom surface of the trench (15) lies above the lowest part of the downward portion of the P layer (20) which is heavily doped
electrically conducting semiconductor material positioned within the trench;	poly gate material (18) in trench (15)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide film (17)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate electrode (18), source electrode (9) and drain electrode (24)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**JP 63-224260**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VMOS FET See fig. 1
providing a first region of a first conductivity type;	N- layer (12).
providing a second region of a second conductivity type over said first region;	P layer (16) and (20)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (14) lying above the P layer (16)
providing a trench through said third and second regions; and	trench (15) extends through N+ layer (17) and P layer (16)
providing a gate in said trench;	poly gate (18)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion of the P layer (20) is laterally spaced from the trench (15) and extends deeper than the trench (15)

CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	a portion P of the P layer is P+ (20) and is doped heavier than the portion (26) of the P layer adjacent the trench (15)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N/A
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	N/A
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide film (17)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 1.
providing a first region of a first conductivity type;	P substrate (11)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (12)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (13) and (20)
providing a fourth region of said first conductivity type over said third region;	N+ layer (14) lying above P layer (13)
providing a trench through said fourth region and third regions; and	trench (15) extending through N+ layer (13) and P layer (13)
providing a gate in said trench;	poly gate (18)
wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the P layer (20) is laterally spaced from trench (15)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (20) and the P layer (11) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (12) and the P layer (20) at the deepest part of the P layer (20) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the third region is P+ (20) which is doped heavier than the part of the third region adjacent the trench (15)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**JP 59-181668**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET See fig. 3
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (11) and (12)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (13)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (14) and (16) lying on N layer (13)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (15) lying partly over the P layer (14), wherein a portion of the P layer is a heavily doped P+ (16) and extends vertically upward through the N+ layer (15) and vertically downward into the N layer (13)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (21) having a bottom surface and side surface and extending vertically downward through the N+ layer (15), the P layer (14) and through a portion of the N layer (13), wherein the bottom surface of the trench (21) lies above the lowest part of the P layer (16).
electrically conducting semiconductor material positioned within the trench;	poly gate in trench (19)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide layer (17)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate electrode (19), source electrode (20) and drain electrode (not shown)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**JP 59-181668**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VMOS FET See fig. 3
providing a first region of a first conductivity type;	N+ layer (11) and (12), and N layer (13)
providing a second region of a second conductivity type over said first region;	P layer (14) and (16) lying on N layer (13)

providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (15) lying wherein N layer (13) and N+ layer (15) are separated by P layer (14)
providing a trench through said third and second regions; and	trench (21) extending vertically downward through the N+ layer (15) and P layer (14)
providing a gate in said trench;	poly gate in trench (19)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion of the P layer (16), which is spaced from the trench, extends deeper than the trench (21)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	a portion of the P layer (14) is a heavily doped P+ (16) which is laterally spaced from the trench (21)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (11) and (12) under N layer (13)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanched breakdown is a reach-through breakdown across the N layer (13)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide layer (17)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 3
providing a first region of a first conductivity type;	N+ layer (11) and (12)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (13)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (14) and (16) lying on N layer (13)
providing a fourth region of said first conductivity type over said third region;	N+ layer (15) lying over the P layer (14)
providing a trench through said fourth region and third regions; and	trench (21) extending vertically downward through the N+ layer (15) and P layer (14)
providing a gate in said trench;	gate oxide layer (17)
wherein a deepest part of said third regions is laterally spaced from said trench;	a portion of the P layer (16) is laterally spaced from the trench (21)

wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (16) and the N+ layer (12) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (13) and the P layer (16) at the deepest part of the P layer (16) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the third region is P+ region (16) which is doped heavier than P region (14) adjacent the trench (21)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 54-57871
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET See fig. 2
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (3) and (10)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (4) lying partly over the P layer (3), wherein a portion of the P layer is a heavily doped P+ (10) and extends vertically upward through the N+ layer (4) and vertically downward into the N layer (2)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (11) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (4), the P layer (3) and through a portion of the N layer (2), wherein the bottom surface of the trench (11) lies above the lowest part of the P layer (10)
electrically conducting semiconductor material positioned within the trench;	Al gate (6) in trench (11)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide layer (5)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate electrode (6), source electrode (7) and drain electrode (9)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**JP 54-57871**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VMOS FET See fig. 2
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (3) and (10).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (4) lying above the P layer (3).
providing a trench through said third and second regions; and	the trench (11) extends through the N+ layer (4) and the P layer (3)
providing a gate in said trench;	Al gate (6) in trench (11)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (10) extends upward through the N+ layer (17) and which extends downward through the N- layer (12)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	a portion P of the second region (10) is doped heavier than another portion (3) of the second region which is adjacent the trench (11)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (1) under N layer (2)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across N layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide layer (5)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 2
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (2)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3) and (10)

providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (3)
providing a trench through said fourth region and third regions; and	trench (11) through N+layer (4) and P layer (3)
providing a gate in said trench;	gate oxide film (5)
wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (10) is laterally spaced from trench (11)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (10) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer (10) at the deepest part of the P layer (10) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the third region (10) is doped heavier than part (3) which is adjacent the trench (11)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 57-72365
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET See fig. 1
a substrate of semiconductor material of heavily doped first electrical conductivity type;	P+ substrate (1)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (3) and (4)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (5) lying partly over the P layer (4), wherein the P layer is heavily doped P+ and extends both vertically upward through the N+ layer (5) and downward into the N layer (2)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (6) having a bottom surface and side surfaces and extending vertically through the N+ layer (5) and the P layer (4), and through a portion of the N layer (2), where the bottom surface of the trench (6) lies above the lowest part of the P layer (3)
electrically conducting semiconductor material positioned within the trench;	metal layer (8)

a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide (7)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate electrode (8), source electrode (9) and drain (D)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 57-72365
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VMOS FET See fig. 1
providing a first region of a first conductivity type;	N layer (2)
providing a second region of a second conductivity type over said first region;	P layer (4) lying over said N layer (2)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (5) lying above the P layer (4)
providing a trench through said third and second regions; and	trench (6) through the N+ layer (5) and the P layer (4)
providing a gate in said trench;	metal gate layer (8)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion of the P layer (3) is spaced from the trench (6) and extends deeper than trench (6)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	a portion of the second region is doped P+ (3) which is heavier doped than another portion of the second region that is adjacent the trench (6)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	P+ layer (1) under N layer (2)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide (7)

CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 1
providing a first region of a first conductivity type;	
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (2)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (4)
providing a fourth region of said first conductivity type over said third region;	N+ layer (5) lying above the P layer (4)
providing a trench through said fourth region and third regions; and	trench (6) through the N+ layer (5) and the P layer (4).
providing a gate in said trench;	metal gate layer (8)
wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the P layer (3) is laterally spaced from trench (6)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (3) and the P+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the third region is doped P+ (3) which is heavier doped than the part of the third region (4) adjacent the trench (6)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 59-193064
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET See fig. 2
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (3)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (4)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top	N+ layer (5) lying partly over the P layer (4), a portion of the P layer (4) extending vertically upward through the N+ layer (5) and downward into the N layer (3)

surface of the third covering layer and a downward portion extending downward into the first covering layer;	
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (1) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (5), the P layer (4) and a portion of the N layer (3), where the bottom surface of the trench (10 lies above the lowest portion of the P layer (4)
electrically conducting semiconductor material positioned within the trench;	gate semiconductor material (8) in trench (1)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide (2)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate (8), source (7) and drain (6)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**JP 59-193064**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 2
providing a first region of a first conductivity type;	N+ layer and N layer (3)
providing a second region of a second conductivity type over said first region;	P layer (4) over N layer (3)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (5) lying above the P layer (4).
providing a trench through said third and second regions; and	trench (1) through N+ layer (5) and P layer (4)
providing a gate in said trench;	gate semiconductor material (8)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion of the P layer (4) is spaced from trench (1) and extends deeper than trench (1)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	obvious to have the second region with a heavier doped P+ portion

CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer under N- layer (3)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer (3)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide (2)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 2
providing a first region of a first conductivity type;	N+ layer
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (3) lying above the N+ layer
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (4)
providing a fourth region of said first conductivity type over said third region;	N+ layer (5) lying above the P layer (4)
providing a trench through said fourth region and third regions; and	trench (1) through the N+ layer (5) and P layer (4)
providing a gate in said trench;	gate oxide (2)
wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of P layer (4) is laterally spaced from trench (1)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (4) and the N+ layer is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (3) and the P layer (4) at the deepest part of the P layer (4) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (1)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 60-28271
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOSFET See fig. 3(a-h)
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)

a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (8) and (11)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (9) lying partly over the P layer (8), where a portion of the P layer (11) extends vertically upward through the N+ layer
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (10) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (9) and the P layer (8) and through a portion of the N layer (2)
electrically conducting semiconductor material positioned within the trench;	poly gate (6) in trench (10)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide film (5)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate (6), source (14) and drain (backside)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442 CLAIM 17	JP 60-28271
17. A method for providing a transistor, said method comprising the steps of :	VMOSFET See fig. 3(a-h)
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (8) and (11).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (9) lying above the P layer (8).
providing a trench through said third and second regions; and	trench (10) through N+ layer (9) and P layer (8)
providing a gate in said trench;	poly gate (6) in trench (10)

wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion P of the second region (11) is spaced from the trench (10); the second region extends deeper than the trench (10)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	portion P of the second region (11) is doped heavier than another portion (8) which is adjacent the trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (1) under N layer (2)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide film (5)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOSFET See fig. 3(a-h)
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (2)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (8)
providing a fourth region of said first conductivity type over said third region;	N+ layer (9) lying above the P layer (8)
providing a trench through said fourth region and third regions; and	trench (10) through N+ layer (9) and P layer (8)
providing a gate in said trench;	poly gate (6) in trench (10)
wherein a deepest part of said third regions is laterally spaced from said trench;	deepest part of the third region is laterally spaced from the trench (10)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (8) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (8) at the deepest part of the P layer (8) and which is reverse biased around its breakdown voltage

CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	obvious to have deepest part of the third region doped heavier than the part adjacent said trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 57-18365
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET See fig. 2
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (3)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (4) lying partly over the P layer (3)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench (5) have a bottom surface and side surfaces which extend vertically downward through the N+ layer (4) and the P layer (3) and through a portion of the N layer (2) in fig. 4, the P layer (2) lies between the N+ layer (4) and the N layer (2) and extends below the bottom surface of the trench (5)
electrically conducting semiconductor material positioned within the trench;	gate (7) in trench (5)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide layer between gate (7) and trench (5)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate (7), source (6) and drain (not drawn)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	JP 57-18365
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	VMOS FET See fig. 2
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (3).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (4) lying above the P layer (3).
providing a trench through said third and second regions; and	trench (5) through N+ layer (4) and P layer (3)
providing a gate in said trench;	gate (7) in trench (5)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (3) extends upward through the N+ layer (4) in fig. 4, P layer (4) extends deeper than trench (5)
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (1)
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (1) under N- layer (2)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer (2)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide layer between gate (7) and trench (5)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	VMOS FET See fig. 2
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (2)

providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3)
providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (3)
providing a trench through said fourth region and third regions; and	trench (5) through N+ layer (4) and P layer (3)
providing a gate in said trench;	gate (7) in trench (5)
wherein a deepest part of said third regions is laterally spaced from said trench;	deepest part of the third region is laterally spaced from the trench (5)
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (7)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	JP 59-80970
CLAIM 1	
1. A trench DMOS transistor cell comprising:	V Groove MOSFET See fig. 2
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (2)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (1)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (8)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	N+ layer (4) lying partly over the P layer (8), where the P layer (8) extends vertically upward through the N+ layer (4) and vertically downward into the N layer (1)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench having a bottom surface and side surface, and extending vertically downward through the N+ layer (4) and the P layer (8) and through a portion of the N layer (1)

electrically conducting semiconductor material positioned within the trench;	gate (6) in trench
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	gate oxide layer (5)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	gate (5), source (7) and drain (not drawn)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**JP 59-80970**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	V Groove MOSFET See fig. 2
providing a first region of a first conductivity type;	N+ layer (2) and N layer (1)
providing a second region of a second conductivity type over said first region;	P layer (8)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (4) lying above the P layer (8)
providing a trench through said third and second regions; and	trench through N+ layer (4) and P layer (8)
providing a gate in said trench;	gate (6) in trench
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	a portion of the P layer (8) is laterally spaced from the trench
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	N+ layer (2) under N- layer (1)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N- layer (1)

CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	gate oxide layer (5)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	V Groove MOSFET See fig. 2
providing a first region of a first conductivity type;	N+ layer (2)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (1)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (8)
providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (8)
providing a trench through said fourth region and third regions; and	V trench extends through the N+ layer (4) and the P layer (3)
providing a gate in said trench;	gate (6) in the V trench
wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the P layer (8) is laterally spaced from the V trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (8) and the N+ layer (2) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (1) and the P layer (8) at the deepest part of the P layer (8) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**U-MOS Power FET, National Technical Report, Vol. 29(2), April 1983**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	U-MOSFET – see Fig. 3 Conceptional fabrication process of U-MOSFET
a substrate of semiconductor material of heavily doped first electrical conductivity type;	n+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	n- layer
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	p layer
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	n+ layer

having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	the p layer includes a p+ portion which extends upward through the n+ layer and downward into the n-layer
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench with a bottom surface and side surfaces which extends downward from the top surface of the n+ layer through the n+ layer, the p layer and through a portion of the n- layer.
electrically conducting semiconductor material positioned within the trench;	semiconductor material within the trench
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide positioned within the trench between the semiconductor material and the bottom and side surfaces of the trench
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the semiconductor material, to the top n+ layer and to the n+ substrate.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	U-MOS Power FET, National Technical Report, Vol. 29(2), April 1983
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	U-MOSFET – see Fig. 3 Conceptional fabrication process of U-MOSFET
providing a first region of a first conductivity type;	n+ layer substrate and n- layer
providing a second region of a second conductivity type over said first region;	p layer
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	n+ layer
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward through the n+ third region, and the p second region
providing a gate in said trench;	gate electrode in the trench
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the p second region has a heavily doped p+ region which is spaced from said trench and extends deeper than said trench

CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	the p second region contains a portion P which is doped heavier than another portion of said second region which is adjacent said trench
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	the first region comprises a n+ layer substrate (first portion) and a n- layer (second portion)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the n- layer (second portion) of the first region
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide positioned within the trench between the semiconductor material and the bottom and side surfaces of the trench
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	U-MOSFET – see Fig. 3 Conceptional fabrication process of U-MOSFET
providing a first region of a first conductivity type;	n+ layer
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	n- layer
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	p layer over n- layer
providing a fourth region of said first conductivity type over said third region;	n+ layer formed over the p layer
providing a trench through said fourth region and third regions; and	trench extending downward through the n+ layer (fourth region) and the p layer (third region)
providing a gate in said trench;	gate electrode in the trench
wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the p layer (third region) is laterally spaced from the trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the p layer (third region) is doped heavier (p+) than the part of the p layer (third region) adjacent the trench

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266 CLAIM 1	**KATOH**
1. A trench DMOS transistor cell comprising:	*Design of New Structural High Breakdown Voltage V-MOSFET—Static Shield V-MOSFET* Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
a substrate of semiconductor material of heavily doped first electrical conductivity type;	n+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	n- layer
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	p layer
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	n+ layer
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	trench extends downward from the top surface of the n+ layer through the n+ layer, the p layer and through a portion of the n- layer.
electrically conducting semiconductor material positioned within the trench;	semiconductor material within the trench
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	oxide positioned within the trench between the semiconductor material and the bottom and side surfaces of the trench
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	three electrodes electrically coupled to the semiconductor material, to the top n+ layer and to the n+ substrate.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**KATOH**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	*Design of New Structural High Breakdown Voltage V-MOSFET—Static Shield V-MOSFET* Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
providing a first region of a first conductivity type;	n+ layer substrate and n- layer
providing a second region of a second conductivity type over said first region;	p layer
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	n+ layer
providing a trench through said third and second regions; and	trench extends through the n+ layer (third region) and the p layer (second region)
providing a gate in said trench;	gate electrode in the trench
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the p second region has a portion which is spaced from said trench and extends deeper than said trench
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	N/A
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	the first region comprises a n+ layer substrate (first portion) and a n- layer (second portion)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the n- layer (second portion) of the first region
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	oxide positioned within the trench between the semiconductor material and the bottom and side surfaces of the trench
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	*Design of New Structural High Breakdown Voltage V-MOSFET—Static Shield V-MOSFET* Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
providing a first region of a first conductivity type;	n+ layer

providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	n- layer
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	p layer over n- layer
providing a fourth region of said first conductivity type over said third region;	n+ layer formed over the p layer
providing a trench through said fourth region and third regions; and	trench extending downward through the n+ layer (fourth region) and the p layer (third region)
providing a gate in said trench;	gate electrode in the trench
wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the p layer (third region) is laterally spaced from the trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	N/A

<u>Prior Art Under 35 U.S.C. § 103 Which Render the '266 and '442 Patents Obvious:</u>

U.S. Patent 4,345,265 in combination with U.S. Patent 4,374,455

U.S. Patent 4,443,931 in combination with U.S. Patent 4,374,455

U.S. Patent 4,532,534 in combination with U.S. Patent 4,374,455

U.S. Patent 4,345,265 in combination with U.S. Patent 4,767,722

U.S. Patent 4,783,694 in combination with U.S. Patent 3,412,297

U.S. Patent 4,593,302 in combination with U.S. Patent 3,412,297

(Multiple alternative combinations using the prior art references combined above can be made which additionally render the '266 and '442 patents obvious)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**U.S. Patent 4,345,265 In Combination With U.S. Patent 4,374,455**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) '455 Patent: Fig. 2: N+ layer (34)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'265 Patent: Figs. 4-6: N- layer (12) '455 Patent: Fig. 2: N- layer (36)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23) '455 Patent: Fig. 2: P layer (52) and (54)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22). '265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (32) and (34) and a downward portion extends downward into the N- layer (12). '455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52) and (54) '455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward in the N- layer (36).
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'455 Patent: Fig. 2: groove (42) having a bottom surface and side surfaces and extending vertically downward from the N+ layer (40) through the N+ layer (40) and the P layer (52) and through a portion of the N- layer (36). '265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point of the grove (42) of the '455 patent
electrically conducting semiconductor material positioned within the trench;	'455 Patent: Fig. 2: electrode (49)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'455 Patent: Fig. 2: oxide layer (47) within the groove (42)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'455 Patent: Fig. 2: source electrodes (58), drain electrode (50) and gate electrode (49).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**U.S. Patent 4,345,265 In Combination With U.S. Patent 4,374,455**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) and N- layer (12) '455 Patent: Fig. 2: N+ layer (34) and N- layer (36)
providing a second region of a second conductivity type over said first region;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23); Col. 3, ln. 42. '455 Patent: Fig. 2: P layer (52) and (54)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22). '455 Patent: Fig. 2: N+ layer (40)
providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	'265 Patent: Col. 5, lns. 32-47 – "The effect of regions 21 and 23 in enhancing the breakdown characteristic of the DMOS structure comes about in several ways. First, the fact that the breakdown occurs at the external periphery of or beneath regions 21 and 22 diverts breakdown from the sensitive channel regions of the DMOS device in the P- regions under the gate 24." '265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point of the grove (42) of the '455 patent
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward in the N- layer (36). '265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; P+ region (21) and (23) are more heavily doped than P- region (20) and (22) near the gate region.
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	'455 patent: Fig. 2: N+ layer (34) under N- layer (36) '265 Patent: Figs. 4-6: N+ layer (10) under N- layer (12)

CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	'265 Patent and '455 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer (12)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	'455 Patent: oxide (47)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) '455 Patent: Fig. 2: N+ layer (34)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'265 Patent: Figs. 4-6: N- layer (12) '455 Patent: Fig. 2: N- layer (36)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23) over the second region '455 Patent: Fig. 2: P layer (52)
providing a fourth region of said first conductivity type over said third region;	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22). '455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52)
providing a trench through said fourth region and third regions; and	'455 Patent: Fig. 2: groove (42) through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
wherein a deepest part of said third regions is laterally spaced from said trench;	'265 Patent: Figs. 4-6: P+ region (21) and (23) is laterally spaced from the gate
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	'265 and '455: a distance between said deepest part of a third region and a first region would be less than a depletion width of a planar junction which has the same doping profile as does said junction between a second and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; P+ region (21) and (23) are more heavily doped than P- region (20) and (22) near the gate region.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**U.S. Patent 4,443,931 In Combination With U.S. Patent 4,374,455**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'931 Patent: Fig. 13: N+ layer (12) '455 Patent: Fig. 2: N+ layer (34)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'931 Patent: Fig. 13: N layer (14) '455 Patent: Fig. 2: N- layer (36)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'931 Patent: Fig. 13: P layer (34) and (28) '455 Patent: Fig. 2: P layer (52) and (54)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	'931 Patent: Fig. 13: N+ layer (36) partly lying over P layer (34) and (28). '931 Patent: Fig. 13: a portion of the P layer (34) is a heavily doped P+ region (28) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (38) and a downward portion extends downward into the N layer (14). '455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52) and (54) '455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward to the N- layer (36).
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'455 Patent: Fig. 2: groove (42) having a bottom surface and side surfaces and extending vertically downward from the N+ layer (40) through the N+ layer (40) and the P layer (52) and through a portion of the N- layer (36).
electrically conducting semiconductor material positioned within the trench;	'455 Patent: Fig. 2: electrode (49)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'455 Patent: Fig. 2: oxide layer (47) within the groove (42)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'455 Patent: Fig. 2: source electrodes (58), drain electrode (50) and gate electrode (49).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**U.S. Patent 4,443,931 In Combination With U.S. Patent 4,374,455**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'931 Patent: Fig. 13: N+ layer (12) and N layer (14) '455 Patent: Fig. 2: N+ layer (34) and N- layer (36)
providing a second region of a second conductivity type over said first region;	'931 Patent: Fig. 13: P layer (34) and (28) '455 Patent: Fig. 2: P layer (52)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	'931 Patent: Fig. 13: N+ layer (12) partly lying over P layer (34) '455 Patent: Fig. 2: N+ layer (40)
providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	'931 patent and '455 patent: the deep P+ region (28) of the '931 patent would be below the lowest point of the grove (42) of the '455 patent
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	'931 Patent: Fig. 13: a portion of the P layer (34) is a heavily doped P+ region (28) '455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward in the N- layer (36).
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	'455 patent: Fig. 2: N+ layer (34) under N- layer (36) '931 Patent: Fig. 13: N+ layer (12) under N- layer (14)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	'931 Patent and '455 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer (12)

CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	'455 Patent: oxide (47)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'931 Patent: Fig. 13: N+ layer (12) '455 Patent: Fig. 2: N+ layer (34)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'931 Patent: Fig. 13: N layer (14) '455 Patent: Fig. 2: N- layer (36)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	'931 Patent: Fig. 13: P layer (34) and (28) '455 Patent: Fig. 2: P layer (52)
providing a fourth region of said first conductivity type over said third region;	'931 Patent: Fig. 13: N+ layer (36) partly lying over P layer (34) and (28) '455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52)
providing a trench through said fourth region and third regions; and	'455 Patent: Fig. 2: groove (42) through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
wherein a deepest part of said third regions is laterally spaced from said trench;	'931 Patent: Fig. 13: P+ region (28) is laterally spaced from the gate
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	'931 and '455: a distance between said deepest part of a third region and a first region would be less than a depletion width of a planar junction which has the same doping profile as does said junction between a second and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	'931 Patent: Fig. 13: a portion of the Player is a heavily doped P+ region (28) and extends both vertically upward and downward; P+ region (28) is more heavily doped than P- region (34) near the gate region.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**U.S. Patent 4,532,534 In Combination With U.S. Patent4,374,455**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'534 Patent: MOSFET With Perimeter Channel '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'534 Patent: Fig. 2: N+ layer (118) '455 Patent: Fig. 2: N+ layer (34)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'534 Patent: Fig. 2: N- layer (120) '455 Patent: Fig. 2: N- layer (36)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'534 Patent: Fig. 2: P layer (124) and (126) '455 Patent: Fig. 2: P layer (52) and (54)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	'534 Patent: Fig. 2: N+ layer (128) partly lying over P layer (124) and (126) '534 Patent: Fig. 2: a portion of the P layer is a heavily doped P+ region (126) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (128) and a downward portion extends downward into the N- layer (120). '455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52) and (54) '455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward to the N- layer (36).
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'455 Patent: Fig. 2: groove (42) having a bottom surface and side surfaces and extending vertically downward from the N+ layer (40) through the N+ layer (40) and the P layer (52) and through a portion of the N- layer (36).
electrically conducting semiconductor material positioned within the trench;	'455 Patent: Fig. 2: electrode (49)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'455 Patent: Fig. 2: oxide layer (47) within the groove (42)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'455 Patent: Fig. 2: source electrodes (58), drain electrode (50) and gate electrode (49).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**U.S. Patent 4,443,534 In Combination With U.S. Patent 4,374,455**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	'534 Patent: MOSFET With Perimeter Channel '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'534 Patent: Fig. 2: N+ layer (118) and N layer (120) '455 Patent: Fig. 2: N+ layer (34) and N- layer (36)
providing a second region of a second conductivity type over said first region;	'534 Patent: Fig. 2: P layer (124) and (126) '455 Patent: Fig. 2: P layer (52)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	'534 Patent: Fig. 2: N+ layer (128) partly lying over P layer (124) and (126) '455 Patent: Fig. 2: N+ layer (40)
providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	'534 patent and '455 patent: the deep P+ region (126) of the '534 patent would be below the lowest point of the grove (42) of the '455 patent
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	'534 Patent: Fig. 12: a portion of the P layer is a heavily doped P+ region (126) '455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward in the N- layer (36).
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	'455 patent: Fig. 2: N+ layer (34) under N- layer (36) '534 Patent: Fig. 2: N+ layer (118) under N- layer (120)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	'534 Patent and '455 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer

CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	'455 Patent: oxide (47)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'534 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion '455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'534 Patent: Fig. 2: N+ layer (118) '455 Patent: Fig. 2: N+ layer (34)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'534 Patent: Fig. 2: N- layer (120) '455 Patent: Fig. 2: N- layer (36)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	'534 Patent: Fig. 2: P layer (124) and (126) '455 Patent: Fig. 2: P layer (52)
providing a fourth region of said first conductivity type over said third region;	'534 Patent: Fig. 2: N+ layer (128) partly lying over P layer (124) and (126) '455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52)
providing a trench through said fourth region and third regions; and	'455 Patent: Fig. 2: groove (42) through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
wherein a deepest part of said third regions is laterally spaced from said trench;	'534 Patent: Figs. 4-6: P+ region (126) is laterally spaced from the gate
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	'534 and '455: a distance between said deepest part of a third region and a first region would be less than a depletion width of a planar junction which has the same doping profile as does said junction between a second and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	'534 Patent: Figs. 4-6: a portion of the P layer is a heavily doped P+ region (126) and extends both vertically upward and downward; P+ region (126) is more heavily doped than P region (124) which is near the gate region.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**U.S. Patent 4,345,265 In Combination With U.S. Patent 4,767,722**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability '722 Patent: Method for Making Planar Vertical Channel DMOS Structures
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) '722 Patent: Figs. 6 and 8: N+ layer (10)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'265 Patent: Figs. 4-6: N- layer (12) '722 Patent: Figs. 6 and 8: N- layer (11)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23) '722 Patent: Figs. 6 and 8: P layer (20a)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22). '265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (32) and (34) and a downward portion extends downward into the N- layer (12). '722 Patent: Figs. 6 and 8: N+ layer (21a) partly lying over P layer (20a)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'722 Patent: Figs. 6 and 8: groove (31) having a bottom surface and side surfaces and extending vertically downward from the N+ layer (21a) through the N+ layer (21a) and the P layer (20a) and through a portion of the N- layer (11). '265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point of the grove (42) of the '455 patent
electrically conducting semiconductor material positioned within the trench;	'722 Patent: Figs. 6 and 8: gate (34)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'722 Patent: Figs. 6 and 8: oxide layer (32) within the groove (31)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'722 Patent: Fig. 6 and 8: source electrodes (50), drain electrode (51) and gate electrode (49).

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	U.S. Patent 4,345,265 In Combination With U.S. Patent 4,767,722
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability '722 Patent: Method for Making Planar Vertical Channel DMOS Structures
providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) and N- layer (12) '722 Patent: Figs. 6 and 8: N+ layer (10) and N- layer (11)
providing a second region of a second conductivity type over said first region;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23); Col. 3, ln. 42. '722 Patent: Figs. 6 and 8: P layer (20a)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22). '722 Patent: Figs. 6 and 8: N+ layer (21a)
providing a trench through said third and second regions; and	'722 Patent: Figs. 6 and 8: groove (31) extending vertically downward through the N+ layer (21a) and the P layer (20a)
providing a gate in said trench;	'722 Patent: Figs. 6 and 8: gate (34) in groove (31)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	'265 Patent: Col. 5, lns. 32-47 – "The effect of regions 21 and 23 in enhancing the breakdown characteristic of the DMOS structure comes about in several ways. First, the fact that the breakdown occurs at the external periphery of or beneath regions 21 and 22 diverts breakdown from the sensitive channel regions of the DMOS device in the P- regions under the gate 24." '265 patent and '722 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point of the grove (31) of the '722 patent
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; P+ region (21) and (23) are more heavily doped than P- region (20) and (22) near the gate region.
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	'722 patent: Figs. 6and 8: N+ layer (10) under N- layer (11) '265 Patent: Figs. 4-6: N+ layer (10) under N- layer (12)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	'265 Patent and '722 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer (11) of the '722 Patent

CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	'722 Patent: oxide (32)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability '722 Patent: Method for Making Planar Vertical Channel DMOS Structures
providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) '722 Patent: Figs. 6 and 8: N+ layer (10)
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'265 Patent: Figs. 4-6: N- layer (12) '722 Patent: Figs. 6 and 8: N- layer (11)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23) over the second region '722 Patent: Figs. 6 and 8: P layer (20a)
providing a fourth region of said first conductivity type over said third region;	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22). '722 Patent: Fig. 6 and 8: N+ layer (21a) partly lying over P layer (20a)
providing a trench through said fourth region and third regions; and	'722 Patent: Figs. 6 and 8: groove (31) through the N+ layer (21a) and the P layer (20a)
providing a gate in said trench;	'722 Patent: Figs. 6 and 8: gate (34)
wherein a deepest part of said third regions is laterally spaced from said trench;	'265 Patent: Figs. 4-6: P+ region (21) and (23) is laterally spaced from the gate
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	'265 and '722: a distance between said deepest part of a third region and a first region would be less than a depletion width of a planar junction which has the same doping profile as does said junction between a second and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; P+ region (21) and (23) are more heavily doped than P- region (20) and (22) near the gate region.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
U.S. Patent 5,072,266	**U.S. Patent 4,783,694 In Combination With U.S. Patent 3,412,297**
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain '297 Patent: MOS Field-Effect Transistor with a One-Micron Vertical Channel
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'694 Patent: Fig. 5: N substrate (40c)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'694 Patent: Fig. 5: N-Epi layer (40) '297 Patent: Figs. 4-6: N layer (10)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'694 Patent: Fig. 5: P layer (42), (42a) and (42e) '297 Patent: Figs. 4-6: P layer (12)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	'694 Patent: Fig. 5: N+ layer (44) partly lying over P layer (42a) and (42e) where a portion of the P layer (42e) is heavily doped P+ and extends vertically upward through the N+ layer (44) and vertically downward into the N-Epi layer (40) '297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'297 Patent: Figs 4-6: trench (18) extends downward from the top surface of the N layer (16) through the N layer (16), P layer (12) and through a portion of the N layer (10)
electrically conducting semiconductor material positioned within the trench;	'297 Patent: conductive semiconductor material (24)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'297 Patent: oxide (14)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'694 Patent: gate (47), source (36) and drain (40c) '297 Patent: electrodes coupled to the gate (24), source (22) and drain (20)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
U.S. Patent No. 5,298,442	**U.S. Patent 4,783,694 In Combination With U.S. Patent 3,412,297**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain '297 Patent: MOS Field-Effect Transistor with a One-Micron Vertical Channel
providing a first region of a first conductivity type;	'694 Patent: Fig. 5: N-Epi layer (40). '297 Patent: Figs. 4-6: N layer (10)
providing a second region of a second conductivity type over said first region;	'694 Patent: Fig. 5: P layer (42), (42a) and (42e) lying over the N-Epi layer (40) '297 Patent: Figs. 4-6: P layer (12)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	'694 Patent: Fig. 5: N+ layer (44) partly lying over P layer (42a) and (42e) '297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
providing a trench through said third and second regions; and	'297 Patent: Figs. 4-6: trench (18) through the N layer (16) and the P layer (12)
providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	'694 patent and '297 patent: the deep P+ region (42e) of the '694 patent would be below the lowest point of the trench (18) of the '297 patent
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	'694 Patent: Fig. 5: a portion of the P layer is a heavily doped P+ region (42e); the P+ region (42e) is doped heavier than the P region (42a) adjacent the gate region.
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	'694 patent: Fig. 5: N+ layer (40c) under N epi layer (40)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	'694 Patent and '297 Patent: avalanche breakdown would be a reach-through breakdown across the N epi layer
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	'297 Patent: oxide (14)

CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain '297 Patent: MOS Field-Effect Transistor with a One-Micron Vertical Channel
providing a first region of a first conductivity type;	
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'694 Patent: Fig. 2: N-Epi layer (40) '297 Patent: Figs. 4-6: N layer (10)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	'694 Patent: Fig. 2: P layer (42), (42a) and (42e) '297 Patent: Figs. 4-6: P layer (12)
providing a fourth region of said first conductivity type over said third region;	'694 Patent: Fig. 2: N+ layer (44) partly lying over P layer (42a) and (42e) '297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
providing a trench through said fourth region and third regions; and	'297 Patent: Figs. 4-6: trench (18) through N layer (16) and P layer (12)
providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
wherein a deepest part of said third regions is laterally spaced from said trench;	'694 Patent: Fig. 5: the deepest part of the P region (42e) is laterally spaced form said trench
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	'694 and '297: a distance between said deepest part of a third region and a first region would be less than a depletion width of a planar junction which has the same doping profile as does said junction between a second and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	'694 Patent: Fig. 5: a portion of the P layer is a heavily doped P+ region (42e) and extends both vertically upward and downward; P+ region (42e) is more heavily doped than P region (42a) which is near the gate region.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266

U.S. Patent 5,072,266	U.S. Patent 4,593,302 In Combination With U.S. Patent 3,412,297
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide '297 Patent: MOS Field-Effect Transistor with a One-Micron Vertical Channel
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'302 Patent: Figs. 20 and 22: N layer (100) '297 Patent: Figs. 4-6: N layer (10)

a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'302 Patent: Figs. 20 and 22: P layer (220) and (221) '297 Patent: Figs. 4-6: P layer (12)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering layer;	'302 Patent: Figs. 20 and22: N+ layer (170) and (171) partly lying over P layer (220) and (221) where a portion of the P layer (220) and (221) is heavily doped P+ and extends vertically upward through the N+ layer (170) and (171) and vertically downward into the N layer (100) '297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'297 Patent: Figs 4-6: trench (18) extends downward from the top surface of the N layer (16) through the N layer (16), P layer (12) and through a portion of the N layer (10)
electrically conducting semiconductor material positioned within the trench;	'297 Patent: conductive semiconductor material (24)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'297 Patent: oxide (14)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'320 Patent: gate (132), source (210) and drain (270) '297 Patent: electrodes coupled to the gate (24), source (22) and drain (20)

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U.S. Patent No. 5,298,442	**U.S. Patent 4,593,302 In Combination With U.S. Patent 3,412,297**
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of :	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide '297 Patent: MOS Field-Effect Transistor with a One-Micron Vertical Channel
providing a first region of a first conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer and N layer (100) '297 Patent: Figs. 4-6: N layer (10)
providing a second region of a second conductivity type over said first region;	'302 Patent: Figs. 20 and 22: P+ layer (220) and (221) lying over the N layer (100) '297 Patent: Figs. 4-6: P layer (12)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171) partly lying over P layer (220) and (221) '297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)

providing a trench through said third and second regions; and	'297 Patent: Figs. 4-6: trench (18) through the N layer (16) and the P layer (12)
providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	'302 patent and '297 patent: the deep P+ region (220) and (221) of the '302 patent would be below the lowest point of the trench (18) of the '297 patent
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	'302 Patent: Figs. 20 and 22: a portion of the P layer is heavily doped P+ region (220) and (221); the P+ region (220) and (221) could be doped heavier than the P region adjacent the gate region.
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	'302 patent: Figs. 20 and 22: N+ layer under N- layer (100)
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	'302 Patent and '297 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer (100)
CLAIM 22	
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate.	'297 Patent: oxide (14)
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide '297 Patent: MOS Field-Effect Transistor with a One-Micron Vertical Channel
providing a first region of a first conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer
providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'302 Patent: Figs. 20 and 22: N layer (100) '297 Patent: Figs. 4-6: N layer (10)
providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	'302 Patent: Figs. 20 and 22: P layer (220) and (221) '297 Patent: Figs. 4-6: P layer (12)
providing a fourth region of said first conductivity type over said third region;	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171) partly lying over P layer (220) and (221) '297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
providing a trench through said fourth region and third regions; and	'297 Patent: Figs. 4-6: trench (18) through N layer (16) and P layer (12)
providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)

wherein a deepest part of said third regions is laterally spaced from said trench;	'302 Patent: Figs 20 and 22: deepest part the third (220) and (221) is laterally spaced from said gate region
wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	'302 and '297: a distance between said deepest part of a third region and a first region would be less than a depletion width of a planar junction which has the same doping profile as does said junction between a second and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	'302 Patent: Figs. 20 and 22: a portion of the P layer is a heavily doped P+ region (220) and (221) and extends both vertically upward and downward; P+ region (220) and (221) could be more heavily doped than P region which is near the gate region.

Fairchild reserves the right to revise and supplement the claim analysis upon further discovery, investigation and analysis prior to the close of discovery. Additionally, the claim construction found by the Court may significantly alter Fairchild's invalidity arguments.

Fairchild asserts that the '266 and '442 patents are invalid under 35 U.S.C. § 112, ¶ 1, as not containing a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention.

Additionally, Fairchild asserts that claim 1 of the '266 and claims 17, 18, 19, 20, 22, 23 and 24 of the '442 patent are invalid as being indefinite under the 35 U.S.C. § 112, ¶ 2. Claim 1 of the '266 and claims 17, 18, 19, 20, 22, 23 and 24 of the '442 patent fail to distinctly claim the subject matter of the invention. For example, the limitation of claim 23 of the '442 patent "wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage" is indefinite under 35 U.S.C § 112, ¶ 2.

Additionally, Fairchild reserves the right to raise a best mode defense upon completion of discovery, specifically upon completion of the depositions of the inventors

In defense of Siliconix's allegation of willful infringement, Fairchild intends to rely upon the opinion(s) of counsel Townsend, Townsend & Crew dated December 23, 1998 and December 8, 1999. Supplemental invalidity/non-infringement opinion(s) will soon be provided to trial counsel.

Dated: August 30, 2000.

TERRENCE P. MCMAHON
WILLIAM L. ANTHONY, JR
MONTE COOPER
KAI TSENG
THOMAS J. GRAY

ORRICK, HERRINGTON & SUTCLIFFE LLP

Kai Tseng
Attorneys for Defendant
FAIRCHILD SEMICONDUCTOR, INC.

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TERRENCE P. McMAHON (State Bar No. 71910)
WILLIAM L. ANTHONY, JR. (State Bar No. 106908)
MONTE COOPER (State Bar No. 196746)
KAI TSENG (State Bar No. 193756)
THOMAS J. GRAY (State Bar No. 191411)
ORRICK, HERRINGTON & SUTCLIFFE LLP
1020 Marsh Road
Menlo Park, CA 94025
Telephone: (650) 614-7400
Facsimile: (650) 614-7401

Attorneys for Defendant,
FAIRCHILD SEMICONDUCTOR

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SILICONIX INCORPORATED, a Delaware corporation Plaintiff, v. FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, Defendant.	CASE NO: C99-04797 SBA **AMENDED INITIAL DISCLOSURE OF DEFENDANT FAIRCHILD SEMICONDUTOR – PRIOR ART PURSUANT TO CIVIL LOCAL RULE 16-7**

I. AMENDED INITIAL DISCLOSURE OF PRIOR ART PURSUANT TO L.R. 16-7(D)

Pursuant to Local Rule 16-7(d), defendant Fairchild Semiconductor Corporation ("Fairchild") makes the following amended initial disclosure of prior art:

Attached hereto is Fairchild's amended initial disclosure of prior art patents, products and publications, and tables categorizing those references. Fairchild's investigation, and its analysis of the listed references, is continuing, and Fairchild reserves the right to supplement and to revise the information provided herein as further analysis is performed, additional information becomes available and discovery is completed. All patents are U.S. patents unless otherwise noted. On information and belief, each listed publication was published at least as early as the date given.

Fairchild incorporates, in full, all references cited (however partially) in the patents-in-suit and/or in their respective file histories, as if fully set forth herein.

While Fairchild will preliminarily identify pursuant to Local Rule 16-7(e) the prior art references which Fairchild believes anticipates the asserted claims or the combination of prior art references which render the asserted claims obvious, please note that the information in this document is provisional and subject to revision, for the following reasons:

(i) Fairchild's position on the invalidity of particular claims will depend on how those claims are construed by the Court. Because claim construction has not yet occurred, Fairchild cannot take a final position on the bases for invalidity of disputed claims because the Court may construe those claims to mean something different from what Fairchild presently assumes them to mean.

(ii) Fairchild's search for prior art is on-going.

(iii) Fairchild has not completed its discovery from Siliconix Inc. Depositions of the persons involved in the drafting and prosecution of the patent-in-suit, and of the inventors, for instance, will likely reveal information that affects the conclusions herein.

II. PRODUCTION OF DOCUMENTS PURSUANT TO L.R. 16-7(F)

As required by Local Rule 16-7(f), Fairchild has already produced technical documentation for the Fairchild FDS6680A, the only product accused of infringement in Siliconix's Claim Chart.

The undersigned certifies that pursuant to local rule 16-6(c) to the best of his knowledge information and belief, formed after a reasonable inquiry, that the disclosure is complete and correct, as of this date.

Dated: August 30, 2000

ORRICK, HERRINGTON & SUTCLIFFE LLP

By: Kai Tseng
Kai Tseng
Attorneys for Defendant
Fairchild Semiconductor Corporation

AMENDED INITIAL DISCLOSURE OF PRIOR ART

U.S. Patents No. 5,072,266 & 5,298,422

SILICONIX INC. VS. FAIRCHILD SEMICONDUCTOR CORPORATION

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
1	Mos Field-Effect Transistor With A One-Micron Vertical Channel	P.R. Amlinger	U.S. PT. NO. 3,412,297	11/19/68	103
2	Integrated Circuit Utilizing Dielectric Plus Junction Isolation	Jean-Claude Frouin et al.	U.S. PT. NO. 3,500,139	03/10/70	103
3	Complementary Field-Effect Transistors On Common Substrate By Multiple Epitaxy Techniques	Roger Cullis	U.S. PT. NO. 3,518,509	06/30/70	103
4	Modified Planar Process For Making Semiconductor Devices Having Ultrafine Mesa Type Geometry	Loyd H. Clevenger	U.S. PT. NO. 3,534,234	10/13/70	
5	Method Of Fabricating Integrated Circuits With Integrated Circuits With Oxidized Isolations And The Resulting Structure	Peltzer	U.S. PT. NO. 3,648,125	03/07/72	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
6	Method Of Manufacturing Semiconductor Devices In Which Silicon Oxide Regions Inset In Silicon Are Formed By A Masking Oxidation, Wherein An Intermediate Layer Of Polycrystalline Silicon Is Provided Between The Substrate And The Oxidation Mask	Appels et al.	U.S. PT. NO. 3,900,350	08/19/75	103
7	Low Capacitance V. Grove Mos Nor Gate And Method Of Manufacture	Rodgers	U.S. PT. NO. 3,924,265	12/02/75	102, 103
8	Multilevel Conductor Structure And Method	Naber	U.S. PT. NO. 3,925,572	12/09/75	103
9	Semiconductor Device Manufacture	Webb	U.S. PT. NO. 3,958,040	05/18/76	
10	Semiconductor Device Having Electrically Insulating Barriers For Surface Leakage Sensitive Devices And Method Of Forming	Abbas et al.	U.S. PT. NO. 3,961,355	06/01/76	
11	Method For Forming Recessed Dielectric Isolation With A Minimized "Birds Beak" Problem	Antipov	U.S. PT. NO. 3,961,999	06/08/76	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
12	Method For Forming Dielectric Isolation Combining Dielectric Deposition And Thermal Oxidation	Feng et al.	U.S. PT. NO. 3,966,514	06/29/76	
13	Dielectrically Isolated Semiconductor Devices	Hochberg	U.S. PT. NO. 3,966,577	06/29/76	
14	Method For Producing A Semiconductor Device And A Semiconductor Device Produced By Said Method	Kooi	U.S. PT. NO. 3,970,486	07/20/76	
15	Method Of Forming Raised Electrical Contacts On A Semiconductor Device	Reichert	U.S. PT. NO. 3,993,515	11/23/76	
16	Method Of Manufacturing A Semiconductor Device Utilizing Monocrystalline-Polycrystalline Growth	Kaji et al.	U.S. PT. NO. 3,977,378	12/14/76	
17	Method For Forming Masks Comprising Silicon Nitride And Novel Mask Structures Produced Thereby	Magdo et al.	U.S. PT. NO. 4,002,511	01/11/77	
18	Single Igfet Memory Cell With Buried Storage Element	Jenne	U.S. PT. NO. 4,003,036	01/11/77	103
19	Field Effect Semiconductor Device	Fukuta	U.S. PT. NO. 4,015,278	03/29/77	
20	Large Value Capacitor	Kendall et al.	U.S. PT. NO. 4,017,885	04/12/77	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
21	Method Of Electrically Isolating Individual Semiconductor Circuits In A Wafer	Nelson et al.	U.S. PT. NO. 4,046,605	09/06/77	
22	Superintegrated V-Grove Isolated Bipolar And Vmos Transistors	Bohn	U.S. PT. NO. 4,048,649	09/13/77	103
23	Fabrication Of Power Field Effect Transistors And The Resulting Structures	Jambotkar	U.S. PT. NO. 4,055,884	11/01/77	
24	Self-Aligned Double Implanted Short Channel V-Grove Mos Device	Ouyang	U.S. PT. NO. 4,065,783	12/27/77	103
25	Vmos Transistor	Wickstrom	U.S. Pt. No. 4,070,690	01/24/78	103
26	Insulated Gate Field Effect Transistor	Ishitani	U.S. PT. NO. 4,072,975	02/07/78	103
27	Field Effect Transistor With A Short Channel Length	Tihani et al.	U.S. PT. NO. 4,101,922	07/18/78	
28	Method For Forming Isolated Regions Of Silicon Utilizing Reactive Ion Etching	Bondur et al.	U.S. PT. NO. 4,104,086	08/01/78	103
29	Epitaxial Method Of Fabricating Single Igfet Memory Cell With Buried Storage Element	Jenne	U.S. PT. NO. 4,105,475	08/08/78	103
30	Semiconductor Memory Device	Masuoka et al.	U.S. PT. NO. 4,115,795	09/19/78	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
31	Method Of Making V-MOS Field Effect Transistor For A Dynamic Memory Cell Having Improved Capacitance	Vinson	U.S. PT. NO. 4,116,720	09/26/78	103
32	Isolation Of Integrated Circuits Utilizing Selective Etching And Diffusion	Murphy et al.	U.S. PT. NO. 4,140,558	02/20/79	103
33	Power Field Effect Transistors	Jambotkar	U.S. PT. NO. 4,145,700	03/20/79	
34	Semiconductor Apparatus	Hendrickson	U.S. PT. NO. 4,148,047	04/03/79	103
35	Method For Fabrication Vertical NPN And PNP Structures Utilizing Ion-Implantation	Anantha et al.	U.S. PT. NO. 4,159,915	07/03/79	
36	High Capacity Dynamic Ram Cell	Tasch, Jr.	U.S. PT. NO. 4,164,751	08/14/79	103
37	Method Of Selective Oxidation In Manufacture Of Semiconductor Devices	Barlett et al.	U.S. PT. NO. 4,170492	10/09/79	
38	VMOS Read Only Memory	Kuo	U.S. PT. NO. 4,198,693	04/15/80	103
39	Semiconductor Memory Device	Natori et al.	U.S. PT. NO. 4,199,772	04/22/80	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
40	Surfacing Process For The Stabilization Of Semiconductor Bodies Employing Glass Containing Quartz Passivating Layer	Chadda	U.S. PT. NO. 4,202,916	05/13/80	103
41	Contact Programmable Double Level Polysilicon MOS Only Memory	Mcelroy	U.S. PT. NO. 4,219,836	08/26/80	
42	VMOS Floating Gate Memory Device	Trotter et al.	U.S. PT. NO. 4,222,062	09/09/80	103
43	VMOS Floating Gate Memory With Breakdown Voltage Lowering Region	Rodgers	U.S. PT. NO. 4,222,063	09/09/80	103
44	Planar Deep Oxide Isolation Process Utilizing Resin Glass And E-Beam Exposure	Lever et al.	U.S. PT. NO. 4,222,792	09/16/80	
45	Random Access MOS Memory Cell Using Double Level Polysilicon	Kuo	U.S. PT. NO. 4,225,945	09/30/80	
46	Vertical Field Effect Transistor With Improved Gate And Channel Structure	Shealy et al.	U.S. PT. NO. 4,262,296	04/14/81	
47	Two-Mask Vj-Fet Transistor Structure	Harrington et al.	U.S. PT. NO. 4,295,267	10/20/81	103
48	Glass-Ceramic Structures And Sintered Multilayer Substrates Thereof With Circuit Patters Of Gold, Silver Or Copper	Kumar et al.	U.S. PT. NO. 4,301,324	11/17/81	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
49	One Device Field Effect Transistor (FET) AC Stable Random Access Memory (Ram) Array	Scheuerlein	U.S. PT. NO. 4,319,342	03/09/82	
50	Method Of Fabricating MOS Field Effect Transistors	Chang et al.	U.S. PT. NO. 4,324,038	04/13/82	
51	Method Of Manufacturing Semiconductor Devices	Iwai et al.	U.S. PT. NO. 4,327,476	05/04/82	
52	Insulated Gate Type Semiconductor Device	Nishizawa	U.S. PT. NO. 4,334,235	06/08/82	
53	Combined DMOS And A Vertical Bipolar Transistor Device And Fabrication Method Therefor	Pao et al.	U.S. PT. NO. 4,344,081	08/10/82	
54	MOS Power Transistor With Improved High-Voltage Capability	Blanchard	U.S. PT. NO. 4,345,265	08/17/82	103
55	Silicon Integrated Circuits	Jaccodine et al.	U.S. PT. NO. 4,353,086	10/05/82	
56	Power MOSFET With An Anode Region	Becke et al.	U.S. PT. NO. 4,364,073	12/14/82	103
57	V-MOS Device With Self-Aligned Multiple Electrodes	Garnache et al.	U.S. PT. NO. 4,364,074	12/14/82	102
58	Semiconductor Integrated Circuit Interconnections	Crowder et al.	U.S. PT. NO. 4,364,166	12/21/82	103
59	Vertical MOSFET With Reduced Turn-On Resistance	Goodman et al.	U.S. PT. NO. 4,366,495	12/28/82	103
60	VMOS Memory Cell And Method For Making Same	Hiltpold	U.S. PT. NO. 4,369,564	12/25/83	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
61	Method For Manufacturing A Vertical, Grooved MOSFET	Goodman	U.S. PT. NO. 4,374,455	02/22/83	102
62	Power Static Induction Transistor Fabrication	Cogan	U.S. PT. NO. 4,375,124	03/01/83	103
63	High Power MOSFET With Low On-Resistance And High Breakdown Voltage	Lidow et al.	U.S. PT. NO. 4,376,286	03/08/83	103
64	Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion	Baliga et al.	U.S. PT. NO. 4,443,931	04/24/84	102, 103
65	Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas	Maydan et al.	U.S. PT. NO. 4,383,885	05/17/83	
66	FET Memory Cell Structure And Process	Fatula Jr. et al.	U.S. PT. NO. 4,397,075	08/09/83	103
67	Fabrication Method For High Power MOS Device	Blanchard et al.	U.S. PT. NO. 4,398,339	08/16/83	103
68	Method For Manufacturing A Field Isolation Structure For A Semiconductor Device	Sakurai	U.S. PT. NO. 4,404,735	09/20/83	103
69	Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions	Herman et al.	U.S. PT. NO. 4,412,242	10/25/83	103
70	Semiconductor Device	Matsumura et al.	U.S. PT. NO. 4,412,237	10/25/83	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
71	Method Of Fabricating Mesa MOSFET Using Overhang Mask	Rice	U.S. PT. NO. 4,419,811	12/13/83	
72	Semiconductor Memory Device	Takei	U.S. PT. NO. 4,432,006	02/14/84	103
73	Enhancement Mode JFET Dynamic Memory	Nishizawa	U.S. PT. NO. 4,434,433	02/28/84	
74	Fabrication of MOS Integrated Circuit Devices	Fuls et al.	U.S. PT. NO. 4,450,620	05/29/84	
75	Isolation For High Density Integrated Circuits	Joy et al.	U.S. PT. NO. 4,454,646	06/19/84	
76	Isolation For High Density Integrated Circuits	Joy et al.	U.S. PT. NO. 4,454,647	06/19/84	
77	Method Of Manufacturing A Self-Aligned U-MOS Semiconductor Device	Iwai	U.S. PT. NO. 4,455,740	06/26/84	103
78	Vertical MESFET With Guardring	Rice	U.S. PT. NO. 4,459,605	07/10/84	
79	Method For Manufacturing VLSI Complementary MOS Field Effect Transistor Circuits In Silicon Gate Technology	Schwabe et al.	U.S. PT. NO. 4,459,740	07/17/84	103
80	Single Electrode U-MOSFET Random Access Memory	Ho et al.	U.S. PT. NO. 4,462,040	07/24/84	103
81	Process For Manufacturing Insulated-Gate Semiconductor Devices With Integral Shorts	Temple	U.S. PT. NO. 4,466,176	08/21/84	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
82	Method For Manufacturing Semiconductor Device	Kameyama	U.S. PT. NO. 4,472,240	09/18/84	103
83	Method Of Fabricating A Bipolar Dynamic Memory Cell	El-Karaeh	U.S. PT. NO. 4,476,623	10/16/84	
84	V-MOS Filed Effect Transistor	David et al.	U.S. PT. NO. 4,503,449	03/05/85	103
85	Method Of Fabricating Power MOSFET Structure Utilizing Self-Aligned Diffusion and Etching Techniques	Vora, et al.	U.S. PT. NO. 4,503,598	03/12/85	103
86	Method For Fabricating Isolation Region In Semiconductor Devices	Goto, et al.	U.S. PT. NO. 4,509,249	04/09/85	
87	Self-Aligned Power MOSFET With Integral Source-Base Short And Methods Of Making	Love	U.S. PT. NO. 4,516,143	05/07/85	103
88	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same	Arnould et al.	U.S. PT. NO. 4,520,552	06/04/85	
89	Method For Forming A Void Free Isolation Structure Utilizing Etch And Refill Techniques	Beyer et al.	U.S. PT. NO. 4,528,047	07/09/85	103
90	MOSFET With Perimeter Channel	Ford et al.	U.S. PT. NO. 4,532,534	07/30/85	103
91	One Transistor Dynamic Random Access Memory	Gibbons	U.S. PT. NO. 4,536,785	08/20/85	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
92	Bidirectional Power With Substrate-Referenced Shield	Schutten et al.	U.S. PT. NO. 4,541,001	09/10/85	103
93	Lateral Bidirectional Notch FET With Extended Gate Insulator	Schutten et al.	U.S. PT. NO. 4,546,367	10/08/85	103
94	Bidirectional Power FET With Field Shaping	Schutten et al.	U.S. PT. NO. 4,553,151	11/12/85	
95		Duplicate			
96	Simplified Planarization Process For Polysilicon Filled Trenches	Shepard	U.S. PT. NO. 4,554,728	11/26/85	
97	Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages	Levinstein et al.	U.S. PT. NO. 4,555,842	12/3/85	
98	Inversion-Mode Insulated-Gate Gallium Arsenide Field-Effect Transistors	Baliga	U.S. PT. NO. 4,568,958	02/03/86	103
99	Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure	Baliga et al.	U.S. PT. NO. 4,571,815	02/25/86	
100	Method of Manufacturing integrated Semiconductor Circuit Devices	Kawakatsu	U.S. PT. NO. 4,582,565	04/15/86	
101	Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide	Lidow, et al.	U.S. PT. NO. 4,593,302	06/03/86	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
102	Power Semiconductor Component And Process For Its Manufacture	Gobrecht et al.	U.S. PT. NO 4,596,999	06/24/86	
103	Vertical Type MOS Transistor	Mihara	U.S. PT. NO 4,608,584	08/24/86	103
104	Lateral Bidirectional Power FET With Notched Multi-Channel Stacking And With Dual Gate Reference Terminal Means	Lade et al.	U.S. PT. NO 4,622,569	11/11/86	103
105	MOS Dynamic Ram	Ogura et al.	U.S. PT. NO 4,630,088	12/16/86	103
106	Method of Fabrication Defect Free Trench Isolation Devices	Hunter et al.	U.S. PT. NO 4,631,803	12/20/86	
107	Process For The Autopositioning Of A Local Field Oxide With Respect To An Insulating Trench	Buiguez et al.	U.S. PT. NO 4,636,281	01/13/87	
108	Vertical MOSFET with Diminished Bipolar Effects	Wheatley, Jr. et al.	U.S. PT. NO 4,639,754	01/27/87	103
109	Method for the manufacture of gate electrodes formed of double layers of metal silicides having a high melting point and doped polycrystalline silicone	Neppl et al.	U.S. PAT NO. 4,640,844	02/03/97	
110	Method for implanting the sidewalls of isolation trenches	Oh et al.	H204	02/03/87	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
111	Dynamic memory device having a single-crystal transistor on a trench capacitor structure and a fabrication method therefor	Lu	U.S. PAT NO. 6,649,625	03/17/87	
112	Shallow grove capacitor fabrication method	Erb et al.	U.S. PAT NO. 4,650,544	03/17/87	
113	Dynamic memory device having a single-crystal transistor on a trench capacitor structure and a fabrication method therefor	Lu	U.S. PAT NO. 4,649,625	03/17/87	
114	Dram cell and array	Malhi	U.S. PAT NO. 4,651,184	03/17/87	103
115	Complementary mos integrated circuits having vertical channel fets	Sunami et al.	U.S. PAT NO. 4,670,768	06/02/87	
116	Semiconductor memory device with trench surrounding each memory cell	Miura et al.	U.S. PAT NO. 4,672,410	06/09/87	103
117	Vertical dram cell and method	Chatterjee et al.	U.S. PAT NO. 4,673,962	06/16/87	103
118	mos transistor	Terry et al.	U.S. PAT NO. 4,675,713	06/23/87	103
119	Process for manufacture of high power mosfet with laterally distributed high carrier density beneath the gate oxide	Lidow et al.	U.S. PAT NO. 4,680,853	07/21/87	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
120	Methods for forming lateral and vertical dmos transistors	Blanchard et al.	U.S. PAT NO. 4,682,405	07/28/87	103
121	Dram cell and array	Chatterjee	U.S. PAT NO. 4,683,486	07/28/87	103
122	Power mos fet with decreased resistance in the conducting state	Mihara	U.S. PAT NO. 4,697,201	09/29/87	
123	Trench etch process	Douglas	U.S. PAT NO. 4,702,795	10/27/87	
124	Method of making trench-incorporated monolithic semiconductor capacitor and high density dynamic memory cells including the capacitor	Goth et al.	U.S. PAT NO. 4,704,368	11/3/87	
125	Passivated dual dielectric gate system and method for fabricating same	Ang et al.	U.S. PAT NO. 4,707,721	11/17/87	
126	Dynamic ram with capacitor groove surrounding switching transistor	Nakamura et al.	U.S. PAT NO. 4,717,942	01/05/88	
127	Trench capacitor process for high density dynamic ram	Baglee et al.	U.S. PAT NO. 4,721,987	01/26/88	
128	Dram with fet stacked over capacitor	Sunami et al	U.S. PAT NO. 4,751,557	06/14/88	
129	High density memory with field shield	Kenney	U.S. PAT NO. 4,751,588	06/14/88	
130		Roger Cullis	United Kingdom 1084937	09/27/67	103
131			France 2.003.068	11/07/69	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
132			Japan 130,178	12/00/76	
133			Japan 53-74385	07/00/78	
134			Fed. Rep. Of Germany 2706155	08/00/78	
135			Japan 0142189	12/00/78	
136			Japan 0149771	12/00/78	
137			Japan 54-885	01/00/79	
138			United Kingdom 2002958	02/00/79	103
139			Japan 039579	03/00/79	
140			Japan 0099583	08/00/79	103
141			Japan 0065463	05/00/80	103
142			Japan 0095366	07/00/80	103
143			Japan 55-146976	11/00/80	103
144			Japan 56-29362	03/00/81	103
145			Japan 0058267	05/00/81	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
146			Japan 0010973	01/00/82	
147			Japan 109367	07/00/82	
148	Dense Vertical FET And Method Of Making	Joseph Shepard	European Pat. Off. 0066081	12/00/82	
149			Japan 0003287	01/00/83	
150			Japan 0010861	01/00/83	
151			Japan 0003269	01/00/83	
152			Japan 141262	02/00/83	
153			Japan 0050752	03/00/83	
154	Curable And Cured Polysulfide Polymer Compositions, Article Manufactured Therefrom And Processes For Preparing The Cured Compositions And Manufactured Articles	Eugene Bertozzi	European Pat. Off. 0008845	09/00/83	
155			Japan 0108325	06/00/84	
156			United Kingdom 2137811A	10/00/84	103
157			Japan 0012752	01/00/85	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
158			Japan 0064444	04/00/85	103
159			Japan 60-154664	08/00/85	103
160			Japan 152059	08/00/85	
161			Japan 0182161	09/00/85	
162			Fed. Rep. Of Germany 3508996	10/00/85	
163			Japan 226165	11/00/85	
164			Japan 261165	12/00/85	
165	Vertical Bidirectional Stacked Power Fet	James Benjamin, et al.	European Patent Off. 0164095	12/00/85	
166	Semiconductor Memory Device	Natsuro Tsubouchi, et al.	United Kingdom 2168195A	12/00/85	
167	Dynamic Ram Cell	Nicky Chau-Chun Lu, et al.	European Pat. Off. 167764	01/00/86	
168			Fed. Rep. Of Germany 3525418	01/00/86	103
169			Japan 36965	02/00/86	
170			Japan 73366	04/00/86	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
171			European Pat. Off. 176254	04/00/86	
172			Japan 61-142774	06/00/86	
173			European Pat. Off. 186875	07/00/86	
174			Japan 198590	11/00/86	
175	"Breakdown Voltage Of Planar Silicon Junctions" from *Solid State Electronics*	O. Leistiko, Jr. and A.S. Grove	N/A	April 15, 1966	
176	"VMOS Memory Technology" from *IEEE International Solid-State Circuits Conference*	Thurman J. Rodgers, Frederick B. Jenne, Bruce Frederick, John J. Barnes, W. Randolph Hiltpold and J. Donald Trotter	N/A	Feb. 16, 1977	103
177	"Recessed Oxide Isolation Process" from *IBM Technical Disclosure Bulletin*	S.A. Abbas	N/A	June, 1977	
178	"VMOS Memory Technology from *IEEE Journal of Solid-State Circuits*	T.J. Rodgers, W. Randy Hiltpold, Bruce Frederick, John J. Barnes, Frederick B. Jenne, James D. Trotter	N/A	Oct. 1977	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
179	"Dynamic DMOS Random-Access Memory Cell Design with Trench" from *IBM Technical Disclosure Bulletin*	F. Barson	N/A	Dec. 1978	103
180	"Fabrication of V-MOS or U-MOS Random-Access Memory Cells With A Self-Aligned Word Line from *IBM Technical Disclosure Bulletin*	T.S. Chang and S. Ogura	N/A	Dec. 1979	103
181	"N. Skin Elimination In UMOS Device By Re-Oxidation from *IBM Technical Disclosure Bulletin*	J.J. Fatula, Jr. and P.L. Garbarino	N/A	Jan. 1980	
182	"Short-Channel Field-Effect Transistors in V-Groves" from *IBM Technical Disclosure Bulletin*	H.S. Lee and R.R. Troutman	N/A	Jan. 1980	103
183	"Vertical FET Random-Access Memories With Deep Trench Isolation" from *IBM Technical Disclosure Bulletin*	T.S. Chang and D.L. Critchlow	N/A	Jan. 1980	103
184	"UMOS Transistors on (110) Silicon from *IEEE Transactions on Electron Devices*	Elie S. Ammar and T.J. Rodgers	N/A	May 1980	103
185	"V-Groove Dynamic Memory Cell" from *IBM Technical Disclosure Bulletin*	D.M. Kenney	N/A	Aug. 1980	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
186	"Reduced BIT Line Capacitance in VMOS Devices from *IBM Technical Disclosure Bulletin*	D.M. Kenney	N/A	Feb. 1981	103
187	"Fabrication of High-Performance LDDFET's with Oxide Sidewall-Spacer Technology	Paul J. Tsang, Seiki Ogura, William W. Walker, Joseph F. Shepard, and Dale L. Critchlow	N/A	April 1982	
188	"CVD Tungsten Interconnect and Contact Barrier Technology for VLSI from *Solid State Technology*	Nicholas E. Miller and Israel Beinglass	N/A	Dec. 1982	
189	"Deep Trench Isolated CMOS Devices" from *IEEE*	R.D. Rung, H. Momose, and Y. Nagakubo	N/A	1982	103
190	"A Half Micron MOSFET Using Double Implanted LDD from *IEEE*	Seiki Ogura, Christopher F. Codella, Nivo Rovedo, Joseph F. Shepard and Jacob Riseman	N/A	1982	
191	"Design, Fabrication, and Evaluation of 2- and 3-Bit GaAs MESFET Analog-to-Digital Converter IC's from *IEEE Transactions on Electron Devices*	L. Chainulu Upadhyayula, Walter R. Curtice, and Rene Smith	N/A	Jan. 1983	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
192	"A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance from *IEEE Transactions on Electron Devices*	Daisuke Euda, Hiromitsu Takagi, and Gota Kano	N/A	Jan. 1984	
193	"The Insulated Gate Transistor: A New Three-Terminal MOS-Controlled Bipolar Power Device from *IEEE Transactions on Electron Devices*	B. Jayant Baliga, Michael S. Adler, Robert P. Love, Peter V. Gray and Nathan D. Zommer	N/A	June 1984	103
194	"Compact One-Device Dynamic Ram Cell With High Storage Capacitance from *IBM Technical Disclosure Bulletin*	C.G. Jambotkar	N/A	July 1984	
195	"Characterization of As-P Double Diffused Drain Structure from *IEDM*	K. Balasubramanyam, M.J. Hargrove, H.I. Hanafi, M.S. Lin, D. Hoyniak, J. LaRue and D.R. Thomas	N/A	1984	
196	"Self-Aligned Titanium Silicidation of Submicron MOS Devices by Rapid Lamp Annealing from *IEDM*	K. Tsukamoto, T. Okamoto, M. Shimizu, T. Matsukawa, and H. Nakata	N/A	1984	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
197	"A High Performance Submicron CMOS Process With Self-Aligned Chan-Stop and Punch-Through Implants (Twin-Tub V) from *IEEE*	M-L. Chen, C-W. Leung, W.T. Cochran, R. Harney, A. Maury and H.P.W. Hey	N/A	1986	
198	"An Ultra-Low On-Resistance Power MOSFET Fabricated by Using a Fully Self-Aligned Process from *IEEE Transaction on Electron Devices*	Daisuke Euda, Hiromitsu Takagi, and Gota Kano	N/A	April 1987	
199	"Self-Aligned UMOSFET's with a Specific On-Resistance of 1 mΩ · cm2 from *IEEE Transactions on Electron Devices*	H..-R Chang, R.D. Black, V.A.K. Temple, Wirojana Tantrapom and B. Jayant Baliga	N/A	Nov. 1987	
200	"Interconnect Materials for VLSI Circuits +	Y. Pauleau	N/A	April 1987	
201	Fabrication Method For High Power MOS Device	Blanchard et al.	4,398,339	08/16/83	103
202	Method For Forming Recessed Isolated Regions	Pliskin et al.	4,506,435	03/26/85	103
203	Grown Side-Wall Silicided Source/Drain Self-Align CMOS Fabrication Process	Alvi et al.	4,764,481	08/16/88	103
204	Method For Making Planar Vertical Channel DMOS Structures	Blanchard	4,767,722	08/30/88	
205	Well Extensions For Trench Devices	Parrillo et al.	4,808,543	02/28/89	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
206	Grooved DMOS Process With Varying Gate Dielectric Thickness	Blanchard	4,914,058	04/03/90	
207	Vertical DMOS Transistor Fabrication Process	Blanchard	4,983,535	01/08/91	
208	Vertical Floating-Gate Transistor	Mori	5,016,068	05/14/91	
209	Method Of Making Topographic Pattern Delineated Power MOSFET With Profile Tailored Recessed	Meyer et al.	5,019,522	05/28/91	
210	Method Of Making A Vertical MOS Transistor	Mori	5,160,491	11/03/92	
211	Integrated MOS Electrical Component	D. Edwards and R. Hofmann	German PT. Off. DE 3028561		
212	Longitudinal Semiconductor Device and Manufacture Thereof	Sasaki Yoshitaka	Japanese PT. Off. JP62037965A	02/18/87	103
213	Manufacture of Vertical Type Semiconductor Device With Groove Section	Sasaki Yoshitaka	Japanese PT. Off. JP62012167A	01/21/87	103
214	Avalanche Injection Into The Oxide In Silicon Gate-Controlled Devices-I Theory From *Solid-State Electronics. 1975 Vol. 18, pp. 363-374*	C. Bulucea	N/A	03/18/74	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
215	Avalanche Injection Into The Oxide In Silicon Gate-Controlled Devices-II Experimental Results From *Solid-State Electronics. 1975 Vol. 18, pp. 381-391*	C. Bulucea	N/A	03/18/74	
216	The Oxidation of Shaped Silicon Surfaces From *Journal of the Electrochemical Society*	R.B. Marcus and T.T. Sheng	N/A	06/00/82	
217	A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance From *IEEE Transactions on Electron Devices, Vol. ED-32, No. 1*	Daisuke Ueda Hiromitsu Takagi and Gota Kano	N/A	01/00/85	103
218	Oxidation of Curved Silicon Surfaces From *Journal of the Electrochemical Society Vol. 134, No. 2*	Lynn O. Wilson and R.B. Marcus	N/A	02/00/87	
219	Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation From *IEEE Transactions On Electron Devices Vol. ED-34, No. 8*	Kikuo Yamabe and Keitaro Imai	N/A	08/00/87	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
220	Self-Aligned UMOSFET's with a Specific On-Resistance of 1mΩ · cm2 From *IEEE Transactions On Electron Devices Vol. ED-34, No. 11*	H.-R. Chang, R.D. Black, V.A.K. Temple, Wirojana Tantraporn and B. Jayant Baliga	N/A	11/00/87	103
221	Breakdown Voltage of Diffused Epitaxial Junctions From *Solid-State Electronics Vol. 34, No. 12 pp. 1313-1318*	Constantin Bulucea	N/A	05/28/91	
222	Process for Manufacture of High Power Mosfet With Laterally Distributed High Carrier Density Beneath the Gate Oxide	Lidow et al.	4,593,302	06/03/86	103
223	Gate Shield Structure For Power Mos Device	Neilson et al.	4,631,564	12/23/86	
224	Semiconductor Device and Method of Manufacturing the Same	Shimizu	4,663,644	05/05/87	103
225	Process for Manufacture of High Power Mosfet With Laterally Distributed High Carrier Density Beneath the Gate Oxide	Lidow et al.	4,680,853	07/21/87	103
226	Method for Making Planar Vertical Channel DMOS Sturctures	Blanchard	4,767,722	08/30/88	102, 103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
227	Static RAM Cell with Trench Pull-Down Transistors and Buried-Layer Ground Plate	Hsu	4,794,561	12/27/88	
228	Method of Making DRAM Cell with Trench Capacitor	Richardson et al.	4,824,793	04/25/89	103
229	Method for Increasing the Performance of Trenched Devices and the Resulting Structure	Blanchard	4,893,160	01/09/90	102, 103
230	Method For Making Planar FET having Gate, Source and Drain In The Same Plane	Lee	U.S. PT NO. 4,685,196	08/11/87	103
231	Method of Making Vertical Dram Cross Point Memory Cell	Lu	U.S. PT NO. 5,362,665	11/08/94	
232	Physics and Technology of Power MOSFETs	S.C. Sun	IDEZ696-1	02/00/82	102, 103
233	Optimization of Discrete High Power MOS Transistors	Richard A. Blanchard	IDEZ696-2	04/00/82	102, 103
234	Various Abstracts of Foreign and Domestic Patents				103
235	Semiconductor Device and Manufacture Thereof	Iwabuchi Toshiyuki and Ochiai Toshiyukl	Japanese PT. Off. 63114173	05/19/88	
236			Japanese PT. Off. 1 – 192174	08/02/89	
237			Japanese PT. Off. 1 – 142775		103
238	Semiconductor Device and Its Preparation	Yasuno Kosuke, et al.	Japanese PT. Off. 56131960 A		103

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239			Japanese PT. Off. 2 – 102579		
240			Japanese PT. Off. 1 - 310576		
241	Semiconductor Device and Manufacture Thereof	Ueda Daisuke, Takagi Hiromitsu, and Kano Kota	Japanese PT. Off. 57-18365 A		103
242			Japanese PT. Off. 60-28271		
243			Japanese PT. Off. 60-28271		103
244	Manufacture of Vertical Type Semiconductor Device with Grove Section	Sasaki Yoshitaka	Japanese PT. Off. 620121167 A		
245	Methods for Forming Lateral and Vertical DMOS Transistors	Blanchard et al.	U.S. PT. No. 4,682,405	07/28/87	103
246	Method of Fabricating Power MOSFET Structure Utilizing Self-Aligned Diffusion and Etching	Vora et al.	U.S. PT. NO. 4,503,598	03/12/85	103
247	Vertical MOSFET and Method of Manufacturing the Same	Morie et al.	U.S. PT. NO. 4,786,953	11/22/88	103
248	FET For High Reserve Bias Voltage and Geometrical Design for Low On Resistance	Hendrickson et al.	U.S. PT. NO. 4,735,914	04/05/88	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
249	Self-Aligned Power MOSFET With Integral Source-Base Short and Methods of Making		U.S. PT. NO. 4,516,143	05/07/85	103
250	Deep Trench Isolated CMOS Devices from *IEEE*	R.D. Rung, H. Momose, and Y. Nagakubo		00/00/82	103
251	1.25 um Deep-Grove-Isolated Self-Aligned Bipolar Circuits from *IEEE*	Denny D. Tang, Paul M. Solomon, Tak H. Ning, Randall D. Isaac, and Rudolph E. Burger		10/00/82	
252	An Advanced High-Performance Trench-Isolated Self-Aligned Bipolar Technology from *IEEE*	G.P. Li, Tak H. Ning, C.T. Chuang, Mark B. Ketchen, Denny Duan-Lee Tang, and John Mauer		11/00/87	103
253	Process and Device Performance of High-Speed Double Poly-Si Bipolar Technology Using Borosenic-Poly Process with Coupling-Base Implant from *IEEE*	Tadanori Yamaguchi, Yeou-Chong Simon Yu, Eric E. Lane, June S. Lee, Evan E. Patton, Robert D. Herman, Diane R. Ahrendt, Vladimir F. Drobny, Todd H. Yuzuriha, and Valdis E. Garuts		08/00/88	
254	A 1um Trench High Speed Bipolar Transistor from *VLSI*	S. Duncan et al.		00/00/88	
255	A Sub-30psec Si Bipolar LSI Technology from *IEEE*	Takayuki Gomi et al.		00/00/88	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
256	Process He: A Highly Advanced Trench Isolated Bipolar Technology For Analogue and Digital Applications	P.C. Hunt and M.P. Cooke		00/00/88	
257	A 0.5 um Very-High-Speed Silicon Bipolar Devices Technology-U-Groove-Isolated SICOS from *IEEE*	Takeo Shiba et al.		11/00/91	
258	MOSAIC V – A Very High Performance Bipolar Technology form *IEEE*	V. dela Torre et al.		00/00/91	
259	A Scaled 0.25-um Bipolar Technology Using Full e-Beam Lithography from *IEEE*	John D. Cressler et al.		05/00/92	
260	A High Performance BICMOS Process Featuring 40 GHz/21 ps from *IEEE*	M. Kerber et al.		00/00/92	
261	A Half-micron Super Self-aligned BiCMOS Technology for High Speed Applications from *IEDM*	T.M. Liu et al.		00/00/92	
262	Bipolar Technology For A 0.5-Micron-Wide Base Transistor With An ECL Gate Delay of 21.5 Picoseconds from *IEDM*	S. Nakamura et al.		00/00/92	
263	Sub-20psec ECL Circuits with 50GHz fmax Self-aligned SiGe HBTs by *IEEE*	Fumihiko Sato, et al.		00/00/92	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
264	Process and Device Characterization for a 30-GHz *f*T Submicrometer Double Poly-Si Bipolar Tehcnology Using BF2-Implanted Base with Rapid Thermal Process from *IEEE*	Tadanori Yamaguchi		08/00/93	
265	0.5 um Bipolar Technology Using a New Base Formation Method: SST1C from *IEEE*	Chikara Yuamaguchi et al.		00/00/93	
266	UHF-1: A High Speed Complementary Bipolar Analog Process on SOI from *IEEE 1992 Bipolar Circuits and Technology Meeting*	C. Davis et al.		00/00/92	
267	CB: A High Speed Complementary Bipolar Process On Bonded SOI from *IEEE 1992 Bipolar Circuits and Technology Meeting*	J.J.J. Feindt et al.		00/00/92	
268	Sub-20 ps High-Speed ECL Bipolar Transistor with Low Parasitic Architecture from *IEEE Transactions on Electron Devices Vol. 42, No. 3*	Toshihiko Iinuma et al.		03/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
269	A 12 Volt Super-Self-Aligned Trench Isolated Complementary Bipolar Technology for Ultra-Low Power and High-Frequency Analog, Mixed Signal and Wireless Applications from *International Technology and Innovation Conference 1995*	Francois Herbert et al.		00/00/95	
270	An Isolation Technology for High Performance Bipolar Memories – IOP-II from *Bipolar Division and *Memory Division, Fujitsu Limited Kawasaki, Kanaagawa, 211 Japan*	Hiroshi Goto, et al.		00/00/00	
271	U-Groove Isolation Technique for High Speed Bipolar VLSI's from *IEEE*	Akio Hayasaka et al.		00/00/82	103
272	A New Trench Isolation Technology As A Replacement of LOCOS from *IEDM*	H. Mikoshiba et al.		00/00/84	
273	A Practical Trench Isolation Technology with a Novel Planarization Process from *IEEE*	G. Fuse, H. Ogawa		00/00/87	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
274	A Variable-Size Shallow Trench Isolation (STI) Technology With Diffused Sidewall Doping For Submicron CMOS from *IEEE*	B. Davari et al.		00/00/88	
275	Double Trench Isolation (DTI): A Novel Isolaiton Technology for Deep-Submicron Silicon Devices from *Advanced Technology Center, Samsung Electronics Co.*	T. Park et al.		00/00/00	
276	Planarized Deep-Trench Process for Self-Aligned Double Polysilicon Bipolar Device Isolation from *J. Electrochem. Soc., Vol. 137, No. 6*	Y.C. Simon et al.		06/00/90	
277	On the Scaling Property of Trench Isolation Capacitance for Advanced High-Performance ECL Circuits from *IEEE Transactions on Electron Devices Vol., 37 No. 10*	P.F. Lu et al.		10/00/90	
278	Trench Isolation Technology from *IEEE 1990 Bipolar Circuits Technology Meeting*	H. Bernhard Pogge et al.		00/00/90	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
279	Framed Mask Poly Buffered LOCOS Isolation for Submicron VLSI Technology from *Advanced Products Research and Development Laboratory*	Bich-Yen Nguyen et al.		00/00/00	
280	Modular Deep Trench Isolation Scheme for 38 GHz Self-Aligned Double Polysilicon Bipolar Devices from *IEEE*	E. Bertagonolli et al.		00/00/91	
281	Improved Shallow Trench Isolation for Sub-Halfmicron CMOS from *Microelectronic Engineering 15 (1991 651-654*	J.P. Cabanal et al.		00/00/91	
282	Optimization of Shallow and Deep Trench Isolation Structures for Ultra-High-Speed Bipolar LSIs from *IEEE 1992 Bipolar Circuits and Technology Meeting*	N Itoh, et al		00/00/92	
283	Deep Trench Isolation for High Voltage Applications from *Motorola Inc., Semiconductor Products Sector*	Francine Y. Robb et al.		00/00/00	

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284	A Highly Manufacturable Trench Isolation Process for Deep Submicron DRAMs from *IEEE*	Pierrce C. Fazan et al.		00/00/93	
285	The Effect of Trench Processing Condition on Complementary Bipolar Analog Devices with SOI/Trench Isolation from *IEEE*	R. Jerome et al.		00/00/93	
286	Offset Trench Isolation from *J. Electrochem. Soc., Vol. 141, No. 8, August 1994*	S.S. Roth		08/00/94	
287	Optimization of a Shallow Trench Isolation Process for Improved Planarization from *J. Electrochem. Soc., Vol. 142 No. 9 September 1995*	S.S. Cooperman et al.		09/00/95	
288	Study of Precipiate-like Defects in CdTe Crystals from *J. Electrochem Soc., Vol 142 No. 9 September 1995*	P. Franzosi, et al.		09/00/95	
289	Platox: A Planarized Trench and Field _IDE Isolation from *International Technology and Innovation Conference 1995*	Rashid Bashir, et al.		00/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
290	Platop: A Novel Planarized Trench Isolation and Field Oxide Formation Using Poly-Silicon from *Analog Process Technology Department, National Semiconductors*	R. Bashir, et al.		00/00/00	
291	Trench Isolation for 0.45 um Active Pitch and Below from *IEEE*	Asanga H. Perera		00/00/95	
292	Silicon Trench Etoch in a Hex Reactor from *Solid State Technology*	G.K. Herb et al.		10/00/87	
293	Optimized High Rate Deep Silicon Trench Etching for Dielectric Isolation in Smart Power Devices from *Siemens AG, Corporate Research and Development Otto-Hahn-Ring 6 D-81730 Munich Germany*	M. Engelhardt		00/00/00	
294	Anisotropic Etching of Silicon Using An SF_6/ Ar Microwave Multipolar Plasma from *J. Vac Sci. technol. B 4 (1)*	C. Pomot et al.		01/00/86 02/00/86	
295	Dry Etching of Silicon Materials in SF_6 Based Plasmas Roles of N_2O and O_2 Additives *J. Electrochem. Soc.: Solid-State Science and Technology*	Y. Tzeng et al.		09/00/87	

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296	RIE Etching of Deep Trenches in Si Ssing $CBrF_3$ and SF_6 Plasma from *Microelectronic Engineering 6 (1987) 553-558*	A.M. Krings et al.		00/00/00	
297	Reactive Ion Etching in SF_6 Gas Mixtures from *J. Electrochem. Soc.,: Solid-State Science and Technology Vol. 134 No. 1*	R. Pinto et al.		01/00/87	
298	Trench Etches in Silicon with Controllable Sidewall Angles from *J. Electrochem. Soc.: Solid-State Science and Technology Vol. 135 No. 8*	Robert N. Carlile et al.		08/00/88	
299	Plasma Etching of Silicon in SF_6 Experimental and Reactor Modeling Studies from *J. Electrochem. Soc., Vol. 137, No. 11*	Yeong-Jyh Lii et al.		11/00/90	
300	Aperture Effect in Plasma Etching of Deep Silicon Trenches from *Vaccum Volume 42/ Numbers 1/2 pages 129 to 131*	M. K. Abachev et al.		00/00/91	
301	Reactive Ion Etching of Silicon Trenches Using SF_6/O_2 Gas Mixtures from *J. Electrochem. Soc., Vol. 138, No. 10*	Tsengyou Syau et al.		10/00/91	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
302	Trench Etching Using a $CBrF_3$ Plasma and Its Study by Optical Emission Spectroscopy by *Vacuum/ Volume 42/Number 14 pages 905 to 910*	G Wohl, et al.		01/14/91	
303	Deep Trench Plasma Etching of Single Crystal Silicon Using SF_6/O_2 Gas Mixtures from *J. Vac. Sci. Technol. B 10(3)*	Christopher P. D'Emic et al.		05/00/92 06/00/92	
304	Reactive Ion Etching of Deep Trenches in Silicon from *584 / SPIE Vol. 1783 International Conference of Microelectronics*	Vladimir N. Bliznetsov		00/00/92	
305	Influences of Reactant Transport on Fluorine Reactive Ion Etching of Deep Trenches in Silicon *J. Vac. Sci. Technol. B 11(6)*	John C. Arnold		11/00/93 12/00/93	
306	Etching of Silicon in $CBrF_3$: Formation of Deep Trenche and Plasma Diagnostics from *386 / SPIE Vol. 1783 International Conference of Microelectronics (1992)*	Yu P. Baryshev et al.		00/00/92	

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307	Deep Trenches in Silicon Using Photoresist As A Mask from *Sensors and Actuators A. 37-38*	E. Cabruja et al.		00/00/93	
308	Rapid Plasma Etching of Silicon, Silicon Dioxide and Silicon Nitride Using Microwave Discharges from *Semicond. Sci. Technol. 8*	S.K. Ray		01/05/93	
309	Highly Anisotropic Selective Reactive Ion Etching of Deep Trenches in Silicon from *Microelectronic Engineering 23*	V.A. Yunkin et al.		00/00/94	
310	The Black Silicon Method: A Universal Method for Determining The Parameter Setting of Fluorine-Based Reactive Ion Etcher in Deep Silicon Trench Etching With Profile Control from *J. Micromech. Microeng. 5*	Henri Jansen et al.		00/00/95	
311	Anisotropic Reactive Ion Etching of Silicon Using $SF_6/O_2/CHF_3$ Gas Mixtures from *J. Electrochem. Soc., Vol. 142 No. 6*	Rob Legtenberg et al.		06/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
312	Deep Trench Fabrication By Si (110) Orientation Dependent Etching from *J. Vac. Sci. Techol. B 13(5)*	Jeremy A. Theil		09/00/95 10/00/95	
313	The Black Silicon Method II: The Effect of Mask Material and Loading On The Reactive Ion Etching Of Deep Silicon Trenches from *Microelectronic Engineering 27 (1995) 475-480*	Henri Jansen et al.		00/00/95	
314	Selectivity and Si-Load In Deep Trench Etching from *Microelectronic Engineering 27 (1995) 457-462*	K. Paul Muller et al.		00/00/95	
315	Silicon Trench Etching Made Easy from *122/Semiconductor International*	Michael Ameen et al.		09/00/88	
316	A Step Coverage and a Hole Filling of Si Film by Surface Reaction Film Formation Technology, from *Abstract No. 190*, pg. 276 - 277	T. Ohmi, M. Kosugi, M. Morita, G.S. Jong, H. Kumagai		00/00/00	
317	Energy and Angular Distribution of Ions Backscattered from the Sidewalls During the Implantation into Deep Trenches, from *Vacuum* Vol. 42, No. 1, 2, pg. 17 - 19	M. Posselt, G. Otto		00/00/91	

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318	Digital Chemical Vapor Deposition of SiO_2 Using a Repetitive Reaction of Triethylsilane/Hydrogen and Oxidation, from *Japanese Journal of Applied Physics* Vol. 30, No. 1B, pg. L124-L127	Hiroyuki Sakaue, Masayuki Nakano, Tsutomu Ichihara, Yasuhiro Horiike		01/00/91	
319	Arsenic Implantation to Oxide Filled Trench Isolation Structure, from *Appl. Phys. Lett* 59 (19), pg. 2400 – 2402	G. Fuse, H. Iwasaki		11/04/91	
320	Submicron Si Trench Profiling With an Electron-Beam Fabricated Atomic Force Microscope Tip, from *Journal of Vacuum Sci. Technology* B 9 (6), pg. 3562 – 3568	Kam L. Lee, David W. Abraham, F. Secord, L. Landstein		11,12/00/91	
321	Pattern Recognition Approach to Trench Bottom-Width Measurement, from *SPIE*, Vol. 1464, *Integrated Circuit Metrology, Inspection, and Process Control V*, pg. 145 – 154	C-H. Chou, J.L. Berman, S.S.C. Chim, T. Corle, G.Q. Xiao, G.S. Kino		00/00/91	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
322	Polysilicon Etchback Plasma Process Using HBr, Cl_2, and SF_6 Gas Mixtures for Deep-Trench Isolation, from *Journal of Electrochemical Society*, Vol. 139, No. 2, pg. 575 - 579	Geun-Young Yeom, Yoshi Ono, Tad Yamaguchi		02/00/92	
323	Conformal Deposition on a Deep-Trenched Subtrate by MOCVD, from *Applied Surface Science*, 70/71, pg. 763 – 767	Yoshihiko Kusakabe, Hiroshi Ohnishi, Toru Takahama, Yoshiyuki Goto		00/00/93	
324	Conformal Deposition on a Deep-Trenched Subtrate by MOCVD, from *Applied Surface Science*, 70/71, pg. 763 – 767 DUPLICATE	Yoshihiko Kusakabe, Hiroshi Ohnishi, Toru Takahama, Yoshiyuki Goto		00/00/93	
325	Digital Chemical Vapor Deposition of Silicon Oxide/Nitride and its Surface Reaction Study, from *Materials Research Society Symp. Proc.*, Vol. 284, pg. 169 – 180	H. Sakaue, T. Nakasako, K. Nakaune, T. Kusuki, A. Miki, Y. Horiike		00/00/93	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
326	Channel-Width Measurements of Locos- and Trench-Isolated MOSFET's by Photoemission, from *IEEE Transactions on Semiconductor Manufacturing*, Vol. 7, No. 3, pg. 259 - 265	Takashi Ohzone, Hideyuk		08/00/94	
327	Nano Trenched Local Oxidation of Silicon Isolation Using Island Polysilicon Grains, from *Journal of Electrochem. Society*, Vol. 143, No. 2, pg. 639 - 642	Sung-Ku Kwon, Chan Lim, Byung-Jin Cho, Jong-Choul Kim		02/00/96	
328	Planarization of Ulsi Topography Over Variable Pattern Densities – pg. 308 – 309	T.H. Doubenspock, C.W. Koburger, J.K. DeBrosse, P.C. Sukanek, M. Armacost, P.C. Buschner, J.A. Abernathey		00/00/00	
329	A New Planarization Technique, Using a Combination of Rie and Chemical Mechanical Polish (CMP), from *IEEE*, pg. 3.4.1 – 3.4.4	B. Davari, C.W. Koburger, R. Schulz, J.D. Warnock, T. Furukawa, M. Jost, Y. Taur, W.G. Schwittek, J.K. DeBrosse, M.L. Kerbaugh, J.L. Mauer		00/00/89	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
330	A Trench Isolation Process for BiCMOS Circuits, from *IEEE 1993 Bipolar Circuits and Technology Meeting 3.3*, pg. 45 – 48	Stephen Poon, Craig Lage		00/00/93	
331	Oxide-Filled Trench Isolation Planarized Using Chemical/Mechanical Polishing	J.M. Pierce, P. Renteln, W.R. Burger, S.T. Ahn		00/00/00	
332	Dishing Effects in a Chemical Mechanical Polishing Planarization Process for Advanced Trench Isolation, from *Appl. Physics Letter 61 (11)* (American Institute of Physics)	C. Yu, P.C. Fazan, V.K. Mathews, T.T. Doan		09/14/92	
333	Chemical/Mechanical Polishing: Emerging Developments in CMP for Semiconductor Planarization, from *Solid State Technology*, pg. 47 - 52	Michael A. Fury		04/00/95	
334	Physical Characterization of Chemical Mechanical Planarized Surface for Trench Isolation, from *Journal of Electrochemical Society*, Vol. 142, No. 9, pg. 3088 – 3092	Iqbal Ali, Mark Rodder, Sudipto R. Roy, Greg Shinn, Mazhar Islam Raja		09/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
335	A Novel Planarization of Trench Isolation Using Polysilicon Refill and Etchback of Chemical-Mechanical Polish, *Journal of Electrochemical Society*, Vol. 142, No. 10, pg. L187 – L188	Yuing-Yi Cheng, Tan Fu Lei, Tien Sheng Chao		10/00/95	
336	Optimization of a Shallow Trench Isolation Refill Process for High Density Non Volatile Memories Using 100% Chemical-Mechanical Polishing. The BOx-ON Process, from Abstract No. 171, pg. 267 - 268	S. Deleonibus, M. Heitzmann, O. Demolliens, Y. Gobil, F. Martin, A.-M. Papon		00/00/00	
337	Decrease in Trenched Surface Oxide Leakage Currents by Rounding off Oxidation, from *Extended Abstracts of the 18 (1986 International) Conference on Solid State Deices and Materials*, pg. 303-306	Keitaro Imai, Kikuo Yamabe		00/00/86	
338	Sidewall Damage in a Silicon Subtrate Caused by Trench Etching, *from Appl. Physics Letter*, 58 (25), pg. 2942 – 2944	Takeshi Hamamoto		06/24/91	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
339	Characterization of the Lateral and Vertical Parasitic Transistors in a Trench Isolated CMOS Process, from Abstract No. 274, pg. 411 - 412	M.C. Roberts, D.J. Foster		00/00/00	
340	Narrow-Width Effects of Shallow Trench-Isolated CMOS with n+-Polysilicon Gate, from *IEEE Transactions on Electron Devices*, Vol. 36, No. 6, pg. 1110 – 1116	Kikuyo Ohe, Shinji Odanaka, Kaori Moriyama, Takashi Hori, Genshu Fuse		06/00/89	
341	A Study of X-Ray Damage Effects on Open-Bottom Trench Isolation for Bipolar Devices, from the *Journal of Electrochemical Society*, Vol. 138, No. 1, pg. 239 – 242	L.C. Hsia		01/00/91	
342	Junction Breakdown Instabilities in Deep Trench Isolation Structures, from *IEEE Transactions on Electron Devices*, Vol. 38, No. 9, pg. 2134 – 2138	Yuk L. Tsang, John M. Aitken		09/00/91	
343	Comparison of Shallow Trench and LOCOS Isolation for Hot-Carrier Resistance, from *IEEE Electron Device Letters*, Vol. 12, No. 12, pg. 673 – 675	Brian S. Doyle, Kaizad R. Mistry		12/00/91	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
344	The Current-Carrying Corner Inherent to Trench Isolation, from *IEEE Electron Device Letters*, Vol. 14, No. 8,mpg. 412 – 414	Andres Bryant, S. Geissler, Jack Mandelman, D. Poindexter, M. Steger		08/00/93	
345	Characterization of Collector-Emitter Leakage in Self-Aligned Double-Poly Bipolar Junction Transistors, from *Journal of Electrochemical Society*, Vol. 140, no. 10, pg. 3033 – 3037	Fanling Yang, Dennis Fuoss, Eric Lane, Tim Archer		10/00/93	
346	Anomalous Narrow Channel Effect in Trench-Isolated Buried-Channel P-MOSFET's, from *IEEE Electron Device Letter*, Vol. 15, No. 12, pg. 496 – 498	J.A. Mandelman, J. Alsmeier		12/00/94	
347	Nonuniform Reverse-Breakdown Characteristics of n+-Diodes Fabricated by LOCOS and Trench Isolation, from *IEEE Transactions on Electron Devices*, Vol. 41, No. 12, pg. 2477 – 2480	Takashi Ohzone, Hideyuki Iwata		12/00/94	
348	Impact of Shallow Trench Isolation on Reliability of Buried- and Surface-Channel sub-*um* PFET, from *IEEE*, pg. 24 – 29	William Tonti, Ronald Bolam, Wilfried Hansch		00/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
349	Process and Device Simulation of Trench Isolation Corner Parasitic Device, from Abstract No. 236, pg. 329 – 330	T. Furukawa, J.A. Mandelman		00/00/00	
350	VIB-2 3D Simulation of Parasitic MOSFET Effects for Box Isolation Technologies, from *IEEE Transactions on Electron Devices*, Vol. 38, No. 12, pg. 3721 – 3722	Gernot Heiser, Matthew Noell, Steve Poon, Marius Orlowski		12/00/91	
351	Efficient Simulation of 3-D Stress Distributions at Trench Structures Caused by Thermal Mismatch of Trench Filling and Silicon Subtrate, from *COMPEL – The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, Vol. 13, no. 4, pg. 861 – 870	R. Slehobr, G. Hobler		00/00/94	
352	Calculation of the Backscattered Ion Energy and Angular Distributions During the Grazing Implantation, from *Vacuum*, vol. 46, No. 4, pg. 383 – 388	I.E. Mozolevsky		00/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
353	Numerical Analysis of a Trench VDMOST Structure with no Quasi-Saturation, from *Solid-State Electronics*, Vol. 38, No. 4, pg. 821 – 828.	J. Zeng, P.A. Mawby, M.S. Towers, K. Boad		00/00/95	
354	Simulation of Film Growth Contour in a Narrow Deep Trench and Film Crystallinity in LPCVD Process, from *Mat. Res. Soc. Symposium Proc.* Vol. 389, pg. 125 – 131	Gyeong Soon Hwang, Chee Burm Shin, San Heup Moonn		00/00/95	
355	Experimental Study and Computer Simulation of Aspect Ratio Dependent Effects Observed in Silicon Reactive Ion Etching, from *Microelectronic Engineering* 30, pg. 345 – 348	V.A. Yunkin, V.F. Lukichev, K.V. Rudenko, D. Fischer, E. Voges		00/00/96	
356	Defect Generation in Trench Isolation, from *IEDM* 84, pg. 586 – 589	Clarence W. Teng, Christopher Slawinski, William R. Hunter		00/00/84	
357	Micro Area Stress Around Trench Structure, from *Extended Abstracts of the 19th Conference on Solid State Devices and Materials*, pg. 327 – 330	S. Nadahara, S. Kambayashi, M. Watanabe, T. Nakakubo		00/00/87	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
358	Stress from Isolation Trenches in Silicon Substrates, from *Journal of Appl. Physics*, 67 (2), pg. 1092 – 1101	S.M. Hu		01/15/90	
359	Oxidation-Induced Defect Generation in Advanced DRAM Structures, from *IEEE Transactions on Electron Devices*, Vol. 37, No. 5, pg. 1253 – 1258	Scott R. Stiffler, Jery B. Lasky, Charles W. Koburger, Wayne S. Berry		05/00/90	
360	Cross Sectional Local Stress-Distribution for Trench Isolation, from *Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials*, pg. 234 – 236	Mamoru Tomozane, Barbara Vasquesz, Teruki Ikeda		00/00/91	
361	Stress Related Problems in Silicon Technology, from *Journal of Appl. Physics*, 70 (6), pg. R53 – R80	S.M. Hu		09/15/91	
362	Residual Stress in Silicon Subtrate with Shallow Trenches on Surface after Local Thermal Oxidation, from *JSME International Journal, Series A.*, Vol. 38, No. 2, pg. 258 – 264	Hideo Miura, Naoto Saito, Hiroyuki Ohta, Noriaki Okamoto		00/00/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
363	Stress Variation Across Arrays of Lines and its Influence on LOCOS Oxidation, from *Microelectronic Engineering* 28, pg. 79-82	I. De Wolf, R. Rooyackers, H.E. Maes		00/00/95	
364	National Trench Isolation Patent Review – presentation materials – Analog/Mixed Signal Process/Device Technology	Wipawan Yindeepol		06/11/96	
365	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Shallow Trench Isolation Process for High Aspect Ratio Trenches	Amitava, Bose, Steven S. Cooperman, Marion M. Garver, Andre I. Nasr	U.S. PAT. No. 5,492,858	02/20/96	
366	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Forming an Isolation Region Comprising a Trench Isolation Region and a Selective Oxidation Film Involved in a Semiconductor Device	Naoya Matsumoto, Junzoh Shimizu	U.S. PAT. No. 5,474,953	12/12/95	
367	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Thermal Trench Isolation	Thomas A. Figura, Nanseng Jeng	U.S. PAT. No. 5;472,904	12/05/95	

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368	Important Trench Patents (06/11/96) -- National Semiconductor – Abstract of Patent : Trench Isolation Structure and Method for Forming	Sudhir K. Madan	U.S. PAT. No. 5,468,676	11/21/95	
369	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Planarized Local Oxidation by Trench-Around Technology; Device Isolation Structure Within a Semiconductor Substrate	Water Lur, Neng H. Shen, Anna Su	U.S. PAT. No. 5,465,003	11/07/95	
370	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Encapsulation Method for Localized Oxidation of Silicon with Trench Isolation	Michael P. Masquelier, Scott S. Roth, Barbara Vasquez	U.S. PAT. No. 5,455,194	10/03/95	
371	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Trench Isolation Stress Relief; Integrated Circuit	Stephen J. Gaul, Donald F. Hemmenway	U.S. PAT. No. 5,448,102	09/05/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
372	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method for Fabricating Semiconductor Device Isolation Using Double Oxide Spacers	Chung-Cheng Wu, Ming-Tzong Yang	U.S. PAT. No. 5,436,190	07/25/95	
373	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Self-Aligned Channel Stop for Trench-Isolated Island	James D. Beasom	U.S. PAT. No. 5,436,189	07/25/95	
374	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Shallow Trench Etch; Semiconductors	Philippe Schoenborn	U.S. PAT. No. 5,413,966	05/09/95	
375	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Simple Planarized Trench Isolation and Field Oxide Formation Using Poly-Silicon	Rashid Bashir, Datong Chen, Francois Herbert	U.S. PAT. No. 5,411,913	05/02/95	
376	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Integrated Circuit With Planarized Shallow Trench Isolation	Fusen E. Chen, Fu-Tai Liou	U.S. PAT. No. 5,410,176	04/25/95	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
377	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Stress-Free Isolation Layer	Water Lur	U.S. PAT. No. 5,395,790	03/07/95	
378	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Manufacturing Trench Isolation	Sung K. Kwon, Hong S. Yang	U.S. PAT. No. 5,387,539	02/07/95	
379	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Planarized Trench and Field Oxide and Poly Isolation Scheme	Rashid Bashir, Datong Chen, Francois Herbert	U.S. PAT. No. 5,385,861	01/31/95	
380	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Locos Technology With Narrow Silicon Trench	Cheng H. Huang, Water Lur	U.S. PAT. No. 5,371,036	12/06/95	
381	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method for Manufacturing Semiconductor Device	Shuichi Harajiri	U.S. PAT. No. 5,348,906	09/20/94	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
382	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Planarization Process for IC Trench Isolation Using Oxidized Polysilicon Filler	Steven S. Cooperman, Andre I. Nasr	U.S. PAT. No. 5,346,584	09/13/94	
383	Important Trench Patents (06/11/96) -- National Semiconductor – Abstract of Patent : Trench Isolation for Both Large and Small Areas by Means of Silicon Nodules after Metal Etching; Local Oxidation by Means of Silicon Nodules After Metal Etching of Aluminum-Silicon Alloy is Achieved	Water Lur, Anna Su, Jiunn Y. Wu	U.S. PAT. No. 5,308,786	05/03/94	
384	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Isolation Technique for Silicon Germanium Devices; Forming Silicon-Germannium layer on Silicon Subtrate, Etching Trench, Forming Silicon Layer and Dielectric Layer on Trench Sidewall	James H. Comfort, David L. Harame, Scott R. Stiffler	U.S. PAT. No. 5,308,785	05/03/94	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
385	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Semiconductor Device Including a Locos Type Field Oxide Film and a U Trench Penetrating the Locos Film	Toru Yamazaki	U.S. PAT. No. 5,306,940	04/26/94	
386	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Process for Simultaneously Fabricating Isolation Structures for Bipolar and CMOS Circuits	Douglas P. Verret	U.S. PAT. No. 5,298,450	03/29/94	
387	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Trench Isolation Process with Reduced Topography	Mark S. Rodder	U.S. PAT. No. 5,223,736	06/29/93	
388	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Forming Island with Polysilicon-Filled Trench Isolation; Forming Silicon Nitride Protective and Polishing Stop Layer, Etching, Stripping to Expose Underlays Oxide Layer	Stephen J. Gaul, Donnald F. Hemmenway	U.S. PAT. No. 5,217,919	06/08/93	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
389	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Trench Isolation Process; Prevent Inversion of Sidewall of Trenches	Guy R. Freeman	U.S. PAT. No. 5,206,182	04/27/93	
390	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : High Density Trench Isolation for MOS Circuits	David Back, Wayne I. Kinney, Jonathan E. Macro, John P. Niemi	U.S. PAT. No. 5,179,038	01/12/93	
391	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Semiconductor Integrated Circuit Device Having Improved Trench Isolation; Surface Grooves of Subtrate are Embedded with Silicon Boron Nitride Dielectric to Isolate Circuit Elements	Mitsuru Sakamott	U.S. PAT. No. 5,168,343	12/01/92	
392	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Semiconductor Device Having Junction Structure of a Plurality of Elemnt. Isolation Regions	Shigeru Morita	U.S. PAT. No. 5,148,258	09/15/92	

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393	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Semiconductor Device Having Trench Isolation	Kazunori Imaoka, Takao Miura	U.S. PAT. No. 5,148,247	09/15/92	
394	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method for Forming Planarized Shallow Trench Isolation in an Integrated Circuit and a Structure Formed Thereby	Fusen E. Chen, Fu-Tai Liou	U.S. PAT. No. 5,130,268	07/14/92	
395	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : High Performance Vertical Bipolar Transistor Structure Via Self-Aligning Processing Techniques; Semiconductors	Gary B. Bronner, David L. Harame, Mark E. Jost	U.S. PAT. No. 5,128,271	07/07/92	
396	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Semiconductor Device with Optimal Distance Between Emitter and Trench Isolation	Mastada Horiuchi, Kiyoji Ikeda, Tohru Nakamura, Kazuo Nakazato, Mitsuo Nanba, Takahiro Onai, Takeo Shiba, Katsuyoshi Washio	U.S. PAT. No. 5,109,263	04/28/92	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
397	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Polysilicon Self-Aligned Bipolar Device Including Trench Isolation and Process of Manufacturing Same; Forming Inlined Isolation Channel in Semiconductor	Jeffrey E. Brighton, Deems R. Hollingsworth, Manuel L. Torreno Jr., Douglas P. Verret	U.S. PAT. No. 5,104,816	04/14/92	
398	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Process for Excavating Trenches with a Rounded Bottom in a Silicon Subtrate for Making Trench Isolation Structures	Pier L. Crotti, Nadia Iazzi	U.S. PAT. No. 5,068,202	11/26/91	
399	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Trench Isolation Process; Filling Groove of Silicon Semiconductor Subtrate having Insulating Sidewalls and Bottom with Polysilicon, Forming, Then Oxidizing the Upper Surface of a Polysilicon Layer Which Extends over the Sidewalls	Clarence W. Teng	U.S. PAT. No. 5,061,653	10/29/91	

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400	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Tapered Trench Structure and Process	Monte A. Douglas	U.S. PAT. No. 5,010,378	04/23/91	
401	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Forming Wide Dielectric-Filled Planarized Isolation Trenches in Semiconductors; Using Silicon Nitride as Etch Stop	Michael L. Kerbaugh, Charles W. Koburger III, Brian J. Macheeney	U.S. PAT. No. 5,006,482	04/09/91	
402	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Manufacturing Semiconductor Devices Using Trench Isolation Method that Forms Highly Flat Buried Insulation Film; Silicon Body with Trenches; Insulation Filling, Masking, Dopes	Kunio Aomura	U.S. PAT. No. 4,988,639	01/29/91	

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403	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Defect Free Trench Isolation Devices and Method of Fabrication; Semiconductors, Insulation, Stress Resistance, Masking, Dielectrics, Field Oxide	William R. Hunter, Christopher Slawinski, Clarence Teng	U.S. PAT. No. 4,983,226	01/08/91	
404	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Fabricating a Semiconductor Device; Trench Isolation Technique to Produce Narrow and Wide Regions	Isamu Namos	U.S. PAT. No. 4,980,311	12/25/90	
405	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Making a CMOS Device with Trench Isolation Devices	Masafumi Shimbo	U.S. PAT. No. 4,980,306	12/25/90	
406	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Manufacturing Semiconductor Device Having Trench Isolation	Nobuyuki Itoh, Hiroomi Nakajima, Hiroyuki Nihira	U.S. PAT. No. 4,931,409	06/05/90	

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407	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Trench Filling; Integrated Circuit Semiconductor Structure	Klaus D. Beyer, Victor J. Silvestri	U.S. PAT. No. 4,924,284	05/08/90	
408	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent : Method of Forming an Oxide Liner and Active Area Mask for Selective Epitaxial Growth in an Isolation Trench	F.J. Robinson	U.S. PAT. No. 4,900,692	02/13/90	
409	Method of Making Vertical Dram Cross Point Memory Cell	Lu	U.S. PT. NO. 5,362,665	11/08/94	
410	Method For Making Planar FET Having Gate, Source And Drain In The Same Place	Lee	U.S. PT. NO. 4,685,196	08/11/87	103
411	Semiconductor Device and Manufacture Thereof (Abstract)	Ajika Natsuo	Japan 63-031170	02/09/88	
412	Semiconductor Device and Manufacture Thereof (Abstract)	Iwabuchi Toshiyuki et al.	Japan 63114173 A	05/19/88	
413			Japan 58-137254	08/15/83	103
414			Japan 62-16572		103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
415	Semiconductor Device and Its Preparation	Yasuno	JP 56-131960 A	10/15/81	103
416	Semiconductor Device and Manufacture Thereof	Ueda	JP 57-018365 A	01/30/82	103
417	Insulated Gate Semiconductor Device	Ashikawa	JP 58-137254 A	08/15/83	102, 103
418	High speed high breakdown voltage Mosfet- has vertical structure with source contact opening extending into gate region	Patel	EP 94891 A	11/23/83	103
419	V-Groove Mos Type Field-Effect Transistor	Yamamoto	JP 59-080970 A	05/10/84	103
420	High Withstand Voltage Vertical Type Transistor Device	Tanaka	JP 59-193064 A	11/01/84	103
421	Vertical Type Mosfet	Tominaga	JP 60-028271 A	02/13/85	103
422	Method of Fabricating Power Mosfet Structure Utilizing Self-Aligned Diffusion and Etching Techniques	Vora	US 4,503,598	03/12/85	103
423	Self-Aligned Power Mosfet with Integral Source-Base Short and Methods of Making	Love	US 4, 516, 143	05/07/85	103
424	DMOS transistor – with body channel and source regions located in substrate	Contiero	EP 179407 (equivalent to US 4,757,032)	04/30/86	103
425			JP 61-142775	06/30/86	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
426	Manufacture of Vertical Type Semiconductor Device with Groove Section -or- Method for Manufacturing Grooved Vertical Semiconductor Device	Sasaki	JP 62-12167 A	01/21/87	102, 103
427	Vertical Type Semiconductor Device and Manufacture Thereof	Sasaki	JP 62-016572 A	01/24/87	102, 103
428	DMOS transistor – with shaped groove providing small area electrical contact	Blanchard	EP 209949 A (equivalent to US 4, 682,405)	01/28/87	103
429	Vertical Type Semiconductor Device and Manufacture Thereof	Sasaki	JP 62-046569 A	02/28/87	103
430	Methods for Forming Lateral and Vertical DMOS Transistors	Blanchard	US 4, 682, 405	07/28/87	103
431	Fet for High Reverse Bias Voltage and Geometrical Design for Low on Resistance	Hendrickson	US 4,735,914	04/05/88	103
432	Semiconductor Device and Manufacture Thereof	Iwabuchi	JP 63-114173 A	05/19/88	102, 103
433	Vertical Mosfet and Method of Manufacturing the Same	Morie	US 4,786,953	11/22/88	103
434			JP 1-192174	08/02/89	103
435			JP 1-310576	12/14/89	103

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436			JP 2-102579	04/16/90	103
437	Insulated gate filed effect transistor	Hideshima et al.	JP 55-146976	11/15/80	102
438	Insulated Gate Semiconductor Device	Ito et al.	JP 58-137254	08/15/83	102
439	Vertical-type Semiconductor Device and Manufacturing Method Therefor	Sasaki	JP 62-16572	01/24/87	102
440	Physics and Technology of Power MOSFETs	Sun		02/00/82	102
441	Optimization of Discrete High Power MOS Transistors	Blanchard		12/00/81	102
442	Method for Manufacturing Grooved Vertical Semiconductor Device	Sasaki	JP 62-12167	01/21/87	102
443	Method for the Formation of Polycrystalline Silicon Layers, and Its Application in the Manufacture of a Self-Aligned, Non Planar, MOS Transistor	Tonnel	U.S. 4,420,379	12/13/83	102
444	Vertical MOSFET	Oshikawa	JP 63-124762	08/15/88	102
445	Conductivity-Modulated MOSFET	Itoh et al.	JP 63-224260	09/19/88	102
446	Semiconductor Device	Nakatani	JP 59-181668	10/16/84	102
447	Semiconductor Device	Okabe et al.	JP 54-57871	05/10/79	102
448	High voltage semiconductor switch	Pernyeszi	JP 57-72365	05/06/82	102

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449	High withstand voltage vertical type transistor device	Tanaka	JP 59-193064	11/01/84	102
450	Vertical MOSFET	Tominaga	JP 60-28271	02/13/85	102
451	Semiconductor Device and Its Method of Manufacture	Ueda et al.	JP 57-18365	01/30/82	102
452	V-groove MOS Field Effect Transistor	Yamamoto	JP 59-80970	05/10/84	102
453	MOS Power Transistor with Improved High-Voltage Capability	Blanchard	U.S. 4,345,265	08/17/82	103
454	Method of Fabricating a Semiconductor Device with a Base Region Having a Deep Portion	Baliga et al.	U.S. 4,443,931	04/24/84	103
455	MOSFET with Perimeter Channel	Ford et al.	U.S. 4,532,534	07/30/85	103
456	Method for Manufacturing a Vertical, Grooved MOSFET	Goodman	U.S. 4,374,455	02/22/83	103
457	MOS-Field Effect Transistor with a One-Micron Vertical Channel	Amlinger	U.S. 3,412,297	11/19/68	103
458	Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain	Merrill et al.	U.S. 4,783,694	11/08/88	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
459	Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide	Lidow et al.	U.S. 4,593,302	06/03/86	103
460	Design of New Structural High Breakdown Voltage V-MOSFET	Katoh et al.		1983	102
461	A Study for High Voltage V-MOS Structure [Japanese]	Kato et al.		1981	102
462	Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect	Kato et al.		1983	102
463	High Voltage-ization Using Static Shield Effect	Kato et al.		1984	102
464	U-MOS Power MOSFET	Ueda et al.		04/00/83	102
465	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Self-aligned, non planar, MOS Transistor	Tonnel	U.S. 4,420,379		
466	Integrated Circuit and Method of Fabrication	Wakefield et al.	U.S. 3,793,721	02/26/74	
467	Gas-Etching Device	Horiike	U.S. 4,192,706	03/11/80	
468	Semiconductor Device with Isolation Between MOSFET and Control Circuit	Takagi et al.	U.S. 4,879,584	11/07/89	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
469	Method of Manufacturing an Insulated Gate Field Effect Transistor	Ueno	U.S. 5,086,007	02/04/92	
470	Power Metal-Oxide-Semiconductor Field Effect Transistor	Yilmaz	U.S. 5,168,331	12/01/92	
471	Low On-Resistance Power MOS Technology	Yilmaz et al.	U.S. 5,304,831	04/19/94	
472	Termination of the Power Stage of a Monolithic Semiconductor Device	Zambrano et al.	U.S. 5,317,182	05/31/94	
473	Bidirectional Power FET with Integral Avalanche Protection	Schutten et al.	U.S. 4,577,208	03/18/86	
474	Bidirectional Power FET with Field Shaping	Schutten et al.	U.S. 4,553,151	11/12/85	
475	Lateral Bidirectional Shielded Notch FET	Schutten et al.	U.S. 4,571,512	02/18/86	
476	High Density, High Voltage Power FET	Benjamin et al.	U.S. 4,571,606	02/18/86	
477	Split Row Power JFET	Benjamin et al.	U.S. 4,635,084	01/06/87	
478	Integrated Gate Field Effect Transistors Having Closed Gate Structure with Controlled Avalanche Characteristics	Dingwall	U.S. 4,173,022	10/30/79	
479			Taiwan 79217	07/16/86	
480			Taiwan 84398	01/16/87	
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